MQ-1100/1132
LCD and Peripheral Controller

Datasheet

Preliminary Version

August 16, 2001

Revision History

The following table constitutes the revisions to this document as of August 16, 2001.

REVISION HISTORY TABLE: Latest Document Revisions

DATE	Chapter	Revision Comments
August 16, 2001	*Chapter 2*	Removed reference to external 3.3V clock oscillator from OSCFO pin.
August 16, 2001	*Chapter 5*	Corrected load current for VOL & VOH spcification.
June 8, 2001	*Formatting updates through-out the datasheet*	The revisions found in this version of the datasheet are the latest revisions for this datasheet.
June 6, 2001	*Chapter 6*	Added figure and table, see *Figure 6-11* anf *Table 6-11.*
June 6, 2001	*Chapter 4*	Changed bit definitions in *Register 4-31* through *Register 4-58*
June 6, 2001	*Chapter 4*	Corrected typogrphic error in *Table 4-8.*
June 6, 2001	*Chapter 5*	Changed specifications in *Table 5-3.*
April 30, 2001	*Chapter 4*	Added Bit Values and Value Definitions to Bit 4:0, *Register 4-75*.
April 30, 2001	*Chapter 2*	Added GPIO6 for Motorola DragonBall 100=pin TQFP number 42, in *Table 2-22.* Changed GPIO values for 132-pin BGA, B3, N3, N4, N14, in *Table 2-22.*
April 30, 2001	*Chapter 4*	Revised section "DMA Transfer and DMA Registers" on page 161.
April 29, 2001	*Revision History Section*	Updated references and links in this section.
April 23, 2001	*Chapter 3*	Revised *Figure 3-8*.
April 23, 2001	*Chapter 2*	Changed descriptions of pin OSCFI and pin OSCFO in *Table 2-2.*
April 23, 2001	*Chapter 4*	Added name to *Register 4-1* through *Register 4-8*. Revised *Section 4.9.1*", General Description and Architecture." Changed *Table 4-7.* . Changed bit definition [2:0] and 6:4] in *Register 4-32*. Added note after *Register 4-74* and *Register 4-82*. Added *Figure 4-4*. Added *Table 4-4.* Changed *Figure 4-1* and *Figure 4-5*.
April 22, 2001	*Chapter 4*	Added Offsets to all the registers. Added *Figure 4-1* and *Figure 4-2*. Revised Bit Definition in *Register 4-2*, bit 10. Revised Section 4.4. Changed *Figure 4-3*.
April 20, 2001	*Chapter 5*	Changed specifications for *Table 5-4.*
April 15, 2001	*Chapter 1*	Added FVSYNC label to *Figure 1-1*.
April 10, 2001	*Chapter 6*	Changed *Figure 6-7*, *Figure 6-8*, *Figure 6-9*, *Figure 6-10* and added specifications to *Table 6-3. Table 6-4. Table 6-5. Table 6-8.* and *Table 6-10.*
April 9, 2001	*Chapter 2*	*Table 2-11.* added MQ-1100 Ball Number for pin UWE#. Changed Type designations in *Table 2-13. Table 2-14. Table 2-18.* and *Table 2-19.*
April 8, 2001	*Chapter 3*	Changed *Figure 3-1* and *Figure 3-8*.
April 8, 2001	*Chapter 4*	Revised section *"Interrupt Controller" on page 79*. Changed figure *"Standard PCI Configuration Space Header Type 00h" on page 83*.
April 4, 2001	*Chapter 5*	Changed and added specifications in *Table 5-4, "DC Characteristics," on page 236.*
April 4, 2001	*Chapter 4*	Added *Register 4-70, "Flat Panel Additional Pin Output Select (FP0BR: Index: 2Ch, Offset 62Ch)," on page 124* Changed *Table 4-2, "Device Configuration Register Index and Reset Values," on page 66.* Bit 10 changed in *Register 4-2, "Device Configuration Register 1 (DC01R: Index 04h, Offset 384h)," on page 67*.
March 30, 2001	*Chapter 6*	Note added after *Table 6-3.* Intel SA11xx Read and after *Table 6-4.* Intel SA11xx Write.
March 30, 2001	*Chapter 5*	*Table 5-3.* Power Dissipation by Function, changed and added values; *Table 5-4.* , changed and added values.
March 30, 2001	*Chapter 4*	*Register 4-5, "Device Configuration Register 4 (DC04R: Index 10h, Offset 390h)," on page 68*, some bits designated as MQ-1132 only; re-wrote section 4.4, Interrupt Controller; re-wrote section 4.7.1; *Register 4-34*, bit 31:26, changed bit definition; *Register 4-31*, bit 27:24, changed bit definition; *Register 4-61*, bit 22, changed value definition. Added textual explanation on page 115. Note added to *Register 4-165, "SPI Module FIFO Threshold Register (SP06R: Index 18h, Offset 318h)," on page 206*.
March 30, 2001	*Chapter 3*	*Figure 3-3*, changed specifications for Graphics Controller Divider 2 Options; added *Figure 3-16*, Generic TFT Timing and accompanying table, see *Table 3-4.*

REVISION HISTORY TABLE: Latest Document Revisions

DATE	Chapter	Revision Comments
March 30, 2001	*Chapter 2*	Changes to *Table 2-2.* (see CGND description); *Table 2-3.* , see Type designation, Pin MD; *Table 2-4.* *Table 2-5.* changed Type description, *Table 2-7.* changed Type description; *Table 2-9.* changed Type description; *Table 2-11.* see Pin LWE#; *Table 2-13.* changed Type description; *Table 2-17.* see Pin BVDD and BGND; *Table 2-22.* (see 100-Pin TQFP).
March 30, 2001	*Chapter 1*	Changes to *Figure 1-1* (see labels and GPIO designations).
March 22, 2001	*Chapter 2*	New pin numbers were added to reflect the MQ-1100 BGA package. New figures were added to correspond to the MQ-1100, 100-pin package.

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Chapter 1

1-1. LCD AND PERIPHERAL CONTROLLER OVERVIEW

The MQ-1100/1132 LCD and Peripheral Controller, is an integrated liquid-crystal display (LCD) and peripheral-interface controller device with embedded memory for low-cost, portable devices that require long battery life and high performance. This single-chip companion integrates key functions supporting a wide range of microprocessor interfaces. It has a high bandwidth, 64-bit wide-memory bus to the embedded SRAM. Featuring scalable bandwidths (up to 192 Mbyte per second), the MQ-1100/1132 offers design flexibility, giving OEMs the opportunity to create their products according to performance and power needs.

Three package options are offered: for the MQ-1100, there is a 100-pin thin quad flat pack (TQFP) package or a 100-pin micro ball grid array (BGA); and for the MQ-1132 there is a 132-pin micro ball-grid array (BGA). These packages make the MQ-1100/1132 family ideal for high-performance, mobile-connected platforms such as personal digital assistants (PDAs), smart phones, tablet computers, and internet appliances. A 2-D graphics engine, LCD display interface, and universal serial bus (USB) Function Controller are integrated on a single chip in either package. Additionally, the 132-pin BGA package includes USB Host Controller, I^2S Audio Codec interface, Serial Peripheral Interface (SPI), support for Peripheral Component Interconnect (PCI) version 2.1, and additional General-Purpose I/O (GPIO) and LED pins.

Figure 1-1 on page 1-2 illustrates the block diagram for MQ-1100/1132.

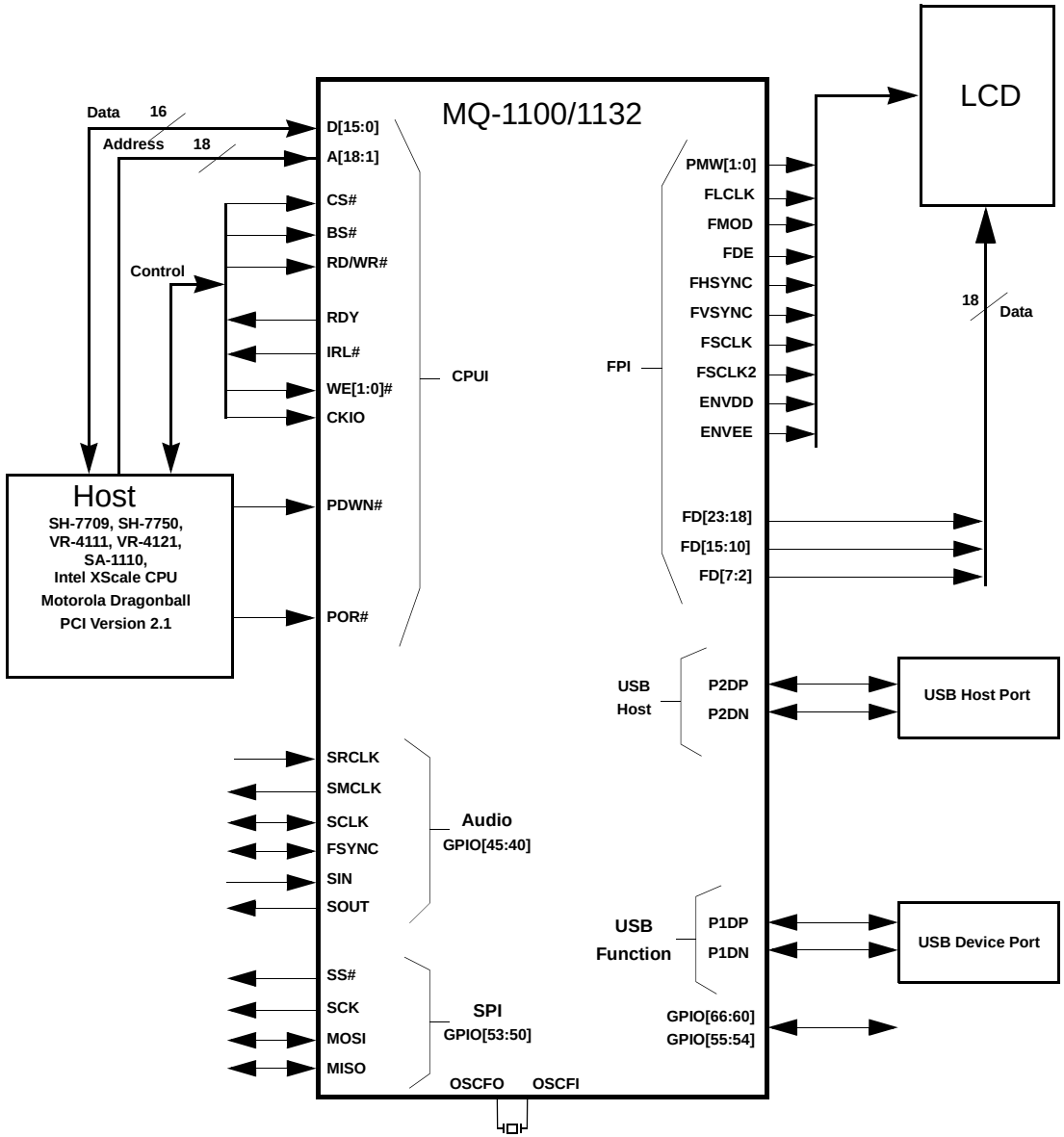


Figure 1-1 MQ-1100/1132 Block Diagram

Chapter 2

2-1. Pin and Package Descriptions

2.2 Pin Descriptions

Table 2-1 specifies the pin types for the MQ-1100/1132 LCD and Peripheral Controller.

TABLE 2-1: MQ-110/MQ-1132 Pin Types

Type	Description
I	CMOS input pin
IS	Schmitt-Trigger CMOS input pin
O	CMOS output pin
I/O	Bi-directional CMOS input/output pin
IS/O	Bi-directional CMOS input/output pin with Schmitt-Trigger CMOS input pin
AP	Analog power (AVDD) pin
AG	Analog ground (AGND) pin
A	Analog pin
AI	Analog input pin
AO	Analog output pin
P	Digital power (VDD) pin
G	Digital ground (GND) pin
OD	Open Drain Output -- pull-up must be provided by the central resource unless noted otherwise

Table 2-1 through *Table 2-20* provide descriptions for the MQ-1100 pins and the MQ-1132 pins.

TABLE 2-2: MQ-1100 and MQ-1132 Clock Pins

Pin Name	Type	MQ-1100 Pin Number	MQ-1100 Ball Number	MQ-1132 Ball Number	Drive (mA)	Description
OSCFI	AI	70	F10	E13	_	**Clock Oscillator Input** When the internal oscillator is selected, an external 48-MHz fundamental mode crystal connected across the OSCFI and OSCFO pins in parallel with a 200K resistor generates the internal clocks. When the internal oscillator is bypassed, this input is tri-stated.
OSCFO	AO	71	E10	E12	_	**Clock Oscillator Output** When the internal oscillator is selected, an external 48-MHz fundamental mode crystal connected across the OSCFI and OSCFO pins in parallel with a 200K resistor generates the internal clocks. When the internal oscillator is bypassed, this input can be driven by an external 1.8 volt clock source.
AVDDO	AP	69	C10	E14	_	**Analog VDD for Oscillator (3.3 V)**
AGNDO	AG	72	A10	D14	_	**Analog GND for Oscillator**

TABLE 2-2: MQ-1100 and MQ-1132 Clock Pins

Pin Name	Type	MQ-1100 Pin Number	MQ-1100 Ball Number	MQ-1132 Ball Number	Drive (mA)	Description
CVDD[4:1]	P	90, 16, 38, 64	A2, G1, K4, G10	A7, H2, M7, H13	_	**Core Power**
CGND[4:1]	G	88, 14, 36, 62	D5, E6, F6, D7	C8, H3, N7, J14	_	**Ground**

TABLE 2-3: MQ-1100 and MQ-1132, Reset and Mode Control Pins

Pin Name	Type	MQ-1100 Pin Number	MQ-1100 Ball Number	MQ-1132 Ball Number	Drive (mA)	Description
POR#	IS	73	C8	D12	_	**Power-On Reset (active low)** Used to reset the MQ-1100/1132. Coming out of reset puts the device in a low-power state where all modules are disabled except for necessary registers.
PDWN# (GPIO4)	IS/O	96	F4	B5	4	**Power Down (active low)** Configured as an input pin during and following power-on reset. The functionality of this pin is determined by the state of the MD[3] pin at the trailing edge of reset. Used as a power-down input pin. Driving low disables the CPU interface input buffers such that external CPU activities will not consume power. **General Purpose I/O** When not used as a power-down pin, it can be used as GPIO 4.
MD3 (GPIO3)	IS/O	97	E4	A4	4	**Mode Select Bit 3** Configured as an input pin during and following power-on reset. The state of this pin is latched with a transparent latch at the trailing edge of the power-on reset pulse. Latched high at the trailing edge of reset, the PDWN# pin is the power-down input pin. If latched low at the trailing edge of reset, the PDWN# pin is a GPIO pin. Typically, a high-impedance pull-down or pull-up resistor is attached to this pin to set the mode. **General Purpose I/O** After reset, this pin can be used as a GPIO pin.
MD2 (GPIO2)	IS/O	98	B6	C4	4	**Mode Select Bit 2** Reserved for an extra mode. Upon reset, this pin is configured with its output buffer tri-stated and its input buffer disabled. **General Purpose I/O** Can be used as GPIO 2.
MD[1:0] (GPIO [1:0])	IS/O	99, 100	D4, D3	A3, A1	4	**Mode Select Bits** These pins are configured as inputs both during and after power-on reset. They are latched with a transparent latch at the trailing edge of the power-on reset pulse to decide the mode of operation. Typically, a high-impedance pull-down or pull-up resistor is attached to this pin to set the mode. **General Purpose I/O** After reset, these pins can be used as GPIO 0 and GPIO 1.

TABLE 2-4: Additional MQ-1132 Reset and Mode Control Pins

Pin Name	Type	MQ-1132 Ball Number	Drive (mA)	Description
PCIMD#, (GPIO5)	IS/O	N14	4	**PCI Mode Select (active low)** Configured as an input both during and after power-on reset. The state of this pin is latched with a transparent latch at the trailing edge of the power-on reset pulse. If latched low at the trailing edge of reset, the PCI bus interface is selected regardless of MD[1:0]. If latched high at the trailing edge of reset, the bus interface is determined by MD[1:0]. Typically, a high-impedance pull-down or pull-up resistor is attached to this pin. **General Purpose I/O Bit 5** This pin can be used as GPIO 5 after reset.

TABLE 2-5: MQ-1100 and MQ-1132, Hitachi SH 7709 and SH 7750 Bus Interface Pins

Pin Name	Type	MQ-1100 Pin Number	MQ-1100 Ball Number	MQ-1132 Ball Number	Drive (mA)	Description
CKIO	IS/O	42	K9	P9	4	**Bus Interface Clock (66 MHz maximum)** Provided by the CPU and used to clock the bus read/write activities. Also used by the CPU for generating the bus interface signals.
BS# (GPIO 7)	IS/O	34	K6	P6	4	**Bus Cycle Start (active low)** Driven by the CPU for one clock to start a bus cycle. **General Purpose I/O Bit 7** This pin can be used as GPIO 7,except for SH3/4 interfaces
CS#	IS	33	K5	N6	_	**Chip Select (active low)** Driven by the CPU to select a MQ-1100/1132 device. The CPU address is only decoded when this signal is asserted.
A[18:1]	IS	13,15, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32	G2, H2, H1, J2, J1, J3, K1, H3, G3, H4, J4, K2, K3, G4, J5, H5, G5, F3	G3, H1, J1, J2, J3, K1, K2, K3, L2, M2, N1, N2, P3, M3, P4, M4, N5, P5	_	**CPU Address Bus** Driven by the CPU for all read/write accesses: 512 Kbyte of address space is provided.
D[15:0]	IS/O	39,40, 45,46, 47,48, 49, 50, 52, 53, 55, 57, 58, 59, 60, 61	J7, J8, J9, H7, H8, H9, G6, G7, G8, G9, J10, E8, F7, F8, F9, H10	M8, P8, P10, N10, M10, N11, N12, P13, M14, M13, L13, L12, K13, K14, K12, J13	8	**CPU Data Bus** Driven by the CPU during write access and by the MQ-1100/1132, LCD and Peripheral Controller during read access. These pins are tri-stated during reset and when the CPU is disabled (powered down).
WE[1:0]#	IS	51, 63	E9, C9	N13, J12	_	**Write Enable Bits (active low)** Byte enables driven by the CPU for write accesses. Ignored for CPU reads which are assumed to be 16-bit accesses.

TABLE 2-5: MQ-1100 and MQ-1132, Hitachi SH 7709 and SH 7750 Bus Interface Pins

Pin Name	Type	MQ-1100 Pin Number	MQ-1100 Ball Number	MQ-1132 Ball Number	Drive (mA)	Description
RD/WR#	IS	35	J6	M6	_	**Read/Write** Driven by the CPU and valid throughout the bus cycle, driven high for read access and driven low for write access.
RDY#, WAIT#	OD	41	K8	N8	PCI	**SH7750 Ready (active low)** Normally pulled-down by an external resistor. The MQ-1100/1132, LCD and Peripheral Controller drives this signal inactive (high) at the appropriate time during CPU read/write access to request additional wait states. After being driven high, RDY# will be driven (low) for one clock then tri-stated. **SH7709 Wait (active low)** Normally pulled-up by an external resistor. The MQ-1100/1132, LCD and Peripheral Controller drives this signal active (low) at the appropriate time during CPU read/write access to request additional wait states. Being driven low, WAIT# will be driven inactive (high) for one clock, then tri-stated.
IRL#	OD	37	H6	P7	4	**Interrupt Request Line (active low)** Interrupt request from the MQ-1100/1132, LCD and Peripheral Controller to the CPU.
BVDD[2:1]	P	44, 54	K7, K10	M9, M12	_	**Bus Interface Power (3.3 V)** Provides power for the bus interface.
BGND[2:1]	G	43, 56	F5, E7	N9, L14	_	**Bus Interface Ground**

TABLE 2-6: Additional MQ-1132, Hitachi SH 7709 and SH 7750, Bus Interface Pins

Pin Name	Type	MQ-1132 Ball Number	Drive (mA)	Description
BVDD[3]	P	P1	_	**Bus Interface Power (3.3 V)**
BGND[3]	G	M1	_	**Bus Interface Ground**

TABLE 2-7: MQ-1100 and MQ-1132 NEC VR-4111 and VR-4121 Bus Interface Pins

Pin Name	Type	MQ-1100 Pin Number	MQ-1100 Ball Number	MQ-1132 Ball Number	Drive (mA)	Description
CS#	IS	33	K5	N6	_	**Chip Select (active low)** Connected to the processor signal LCDCS# and driven by the CPU to select the MQ-1100/1132 for system memory accesses. The CPU address bus is only decoded when this signal is asserted.
A[18:1]	IS	13,15, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32	G2, H2, H1, J2, J1, J3, K1, H3, G3, H4, J4, K2, K3, G4, J5, H5, G5, F3,	G3, H1, J1, J2, J3, K1, K2, K3, L2, M2, N1, N2, P3, M3, P4, M4, N5, P5	_	**CPU Address Bus** Driven by the CPU for all read/write accesses and provides 512 Kbyte of address space.
D[15:0]	IS/O	39,40,45, 46, 47, 48,49, 50, 52, 53, 55, 57, 58, 59, 60, 61	J7, J8, J9, H7, H8, H9, G6, G7, G8, G9, J10, E8, F7, F8, F9, H10	M8, P8, P10, N10, M10, N11, N12, P13, M14, M13,L13, L12, K13, K14, K12, J13	8	**CPU Data Bus** Driven by the CPU during write access and is driven by the MQ-1100/1132, during read access. These pins are tri-stated during reset and when the CPU is disabled (powered down).
BE[1:0]#	IS	51, 63	E9, C9	N13, J12	_	**Byte Enable Bits (active low)** Byte enables driven by the CPU for write accesses to the MQ-1100/1132. Ignored for CPU reads as they are assumed to be 16-bit access. These signals are connected to the processor signals SHBEx# and ADD0#, respectively.
RD#	IS	35	J6	M6	_	**Read Signal (active low)** Driven low by the CPU for read access to the MQ-1100/1132.
WR#	IS	42	K9	P9	_	**Write Signal (active low)** Driven low by the CPU for write access to this MQ-1100/1132.
RDY	OD	41	K8	N8	PCI	**Ready (active high)** Connected to the processor signal LCDRDY and typically pulled-up by an external resistor. The MQ-1100/1132 device drives this signal inactive (low) at the correct time during the CPU read/write access to request additional wait states. After being driven low, the MQ-1100/1132 will drive this signal active (high) for one clock before tri-stating the output buffer.
IRL#	OD	37	H6	P7	4	**Interrupt Request Line (active low)** Interrupt request from the MQ-1100/1132 device to the CPU.
BVDD[2:1]	P	44, 54	K7, K10	M9, M12	_	**Bus Interface Power (3.3 V)**
BGND[2:1]	G	43, 56	F5, E7	N9, L14	_	**Bus Interface Ground**

TABLE 2-8: Additional MQ-1132, NEC VR-4111 and VR-4121 Bus Interface Pins

Pin Name	Type	MQ-1132 Ball Number	Drive (mA)	Description
BVDD[3]	P	P1	_	**Bus Interface Power (3.3 V)**

TABLE 2-8: Additional MQ-1132, NEC VR-4111 and VR-4121 Bus Interface Pins

Pin Name	Type	MQ-1132 Ball Number	Drive (mA)	Description
BGND[3]	G	M1	_	**Bus Interface Ground**

TABLE 2-9: MQ-1100/1132, Intel SA-110 and SA-2 Bus Interface Pins

Pin Name	Type	MQ-1100 Pin Number	MQ-1100 Ball Number	MQ-1132 Ball Number	Drive (mA)	Description
CS#	IS	33	K5	N6	_	**Chip Select (active low)** Driven by the CPU to select the MQ-1100/1132 device. The CPU address bus is only decoded when CS# is asserted.
A[18:1]	IS	13,15, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32	G2,H2,H1, J2, J1, J3, K1, H3, G3, H4, J4, K2, K3, G4, J5, H5, G5, F3	G3, H1, J1, J2, J3, K1, K2, K3, L2, M2, N1, N2, P3, M3, P4, M4, N5, P5	_	**CPU Address Bus** This address bus is driven by the CPU for all read/write accesses and provides 512 Kbyte of address space.
D[15:0]	IS/O	39,40,45, 46, 47, 48,49, 50, 52, 53, 55, 57, 58, 59, 60, 61	J7, J8, J9, H7, H8, H9, G6, G7, G8, G9, J10, E8, F7, F8, F9, H10	M8, P8, P10, N10, M10, N11, N12, P13, M14,M13, L13, L12, K13, K14, K12, J13	8	**CPU Data Bus** Driven by the CPU during write access and the MQ-1100/1132 device during read access. These pins are tri-stated during reset and when the CPU is disabled (powered down).
BE[1:0]#	IS	51, 63	E9, C9	N13, J12	_	**Byte Enable Bits (active low)** Driven by the CPU for write accesses. Since the CPU reads are assumed to be 16-bit accesses, these pins are ignored for the CPU reads.
OE#	IS	35	J6	M6	_	**Output Enable (active low)** Driven low by the CPU for read accesses to the MQ-1100/1132.
WR#	IS	42	K9	P9	_	**Write Signal (active low)** Driven low by the CPU for write accesses to the MQ-1100/1132.
RDY	OD	41	K8	N8	PCI	**Ready (active high)** This signal is typically pulled-up by an external resistor. The MQ-1100/1132 device drives this signal inactive (low) at the appropriate time during CPU read/write access to request additional wait states. After the signal is driven low, it is driven active (high) for one clock before it is tri-stated.
IRL#	OD	37	H6	P7	PCI	**Interrupt Request Line (active low)** Interrupt request from MQ-1100/1132 device to the CPU.
BVDD[2:1]	P	44, 54	K7, K10	M9, M12	_	**Bus Interface Power (3.3 V)**
BGND[2:1]	G	43, 56	F5, E7	N9, L14	_	**Bus Interface Ground**

TABLE 2-10: Additional MQ-1132, Intel SA-1110 XScale CPU Bus Interface Pins

Pin Name	Type	MQ-1132 Ball Number	Drive (mA)	Description
BVDD[3]	P	P1	_	**Bus Interface Power (3.3 V)**
BGND[3]	G	M1	_	**Bus Interface Ground**

TABLE 2-11: MQ-1100/1132, Motorola DragonBall Series Bus Interface Pins

Pin Name	Type	MQ-1100 Pin Number	MQ-1100 Ball Number	MQ-1132 Ball Number	Drive (mA)	Description
CS#	IS	33	K5	N6	_	**Chip Select (active low)** Driven by the CPU to select the MQ-1100/1132 device. The CPU address is only decoded when this signal is asserted. This is connected to the processor signal CS(A1/B0/B1)#.
A[18:1]	IS	13,15, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32	G2, H2, H1, J2, J1, J3, K1, H3, G3, H4, J4, K2, K3, G4, J5, H5, G5, F3	G3, H1, J1, J2, J3, K1, K2, K3, L2, M2, N1, N2, P3, M3, P4, M4, N5, P5	_	**CPU Address Bus** This address bus is driven by CPU for all read/write accesses. This provides 512 Kbyte of address space on each chip-select.
D[15:0]	IS/O	39,40,45,46, 47, 48,49, 50, 52, 53, 55, 57, 58, 59, 60, 61	J7, J8, J9, H7, H8, H9, G6, G7, G8, G9, J10, E8, F7, F8, F9, H10	M8, P8, P10, N10, M10, N11, N12, P13, M14, M13,L13, L12, K13, K14, K12, J13	8	**CPU Data Bus** Driven by the CPU during write access and by the MQ-1100/1132 device during read access. Tri-stated during reset and when the CPU is disabled (powered down).
LWE#	IS	63	E9	J12	_	**Lower Byte Write Enable Bits (active low)** Driven low by the CPU for write access to lower eight bits of data.
UWE#	IS	51	C9	N13	_	**Upper Byte Write Enable Bits (active low)** Driven low by the CPU for write access to upper eight bits of data.
OE#	IS	35	J6	M6	_	**Output Enable (active low)** Driven low by the CPU for read accesses.
DTACK#	OD	41	K8	N8	PCI	**Data Transfer Acknowledge (active low)** An external 10K ohm pull-up resistor on this signal is required. The MQ-1100/1132 device drives this signal low at the appropriate time during CPU read/write accesses to indicate the completion of the data transfer. When the CPU recognizes DTACK# low during a read cycle, data is latched. When the CPU recognizes DTACK# low during a write cycle, the bus cycle is terminated. After it is driven low, it is driven high, then tri-stated.
IRL#	OD	37	H6	P7	4	**Interrupt Request Line (active low)** This is an interrupt request from the MQ-1100/1132 device to the CPU.
GPIO6	!S/O	42	K9	P9	4	**General Purpose I/O** Can serve as GPIO6 with the Motorola Dragonball series bus I/F. Upon reset it can be configured with output tristated and input buffer disabled.
BVDD[2:1]	P	44, 54	K7, K10	M19, M12	_	**Bus Interface Power (3.3V)**
BGND[2:1]	G	43, 56	F5, E7	N9, L14	_	**Bus Interface Ground**

TABLE 2-12: Additional MQ-1132 Motorola DragonBall Series Bus Interface Pins

Pin Name	Type	MQ-1132 Ball Number	Drive (mA)	Description
BVDD[3]	P	P1	_	**Bus Interface Power (3.3 V)**
BGND[3]	G	M1	_	**Bus Interface Ground**

TABLE 2-13: MQ-1132 PCI Bus Interface Pins

Pin Name	Type	MQ-1132 Ball Number	Drive (mA)	Description
CLK	IS	P9	PCI	**Bus Interface Clock (33 MHz maximum)** Driven by the PCI host and used to clock the bus read/write activities. It is also the clock used by the PCI host for generating the bus interface signals.
IDSEL (GPIO22)	IS/O	P14	_	**Initialization Device Select** Driven by the PCI host and used as a chip select during configuration read and write transactions. **General Purpose I/O** When the PCI interface is not used this pin can be configured as a GPIO 22
FRAME#	IS	N6	_	**Frame Signal (active low)** Driven by the PCI host to indicate the beginning and duration of an access.
AD[31:0]	IS/O	J1, J2, J3, K1, K2, K3, L2, M2, N1, N2, P3, M3, P4, M4, N5, P5, M8, P8, P10, N10, M10, N11, N12, P13, M14, M13, L13, L12, K13, K14, K12, J13	8	**Address/Data Bus** Multiplexed address/data bus driven by the PCI host. During the address phase, D[31:2] contains the address of the transaction. During the data phase D[31:0] contains the data.
C/BE3# (GPIO21) C/BE2# (GPIO20) C/BE[1:0]	IS/O	P2 M5 N13, J12	_	**Command Bits (active high) / Byte Enable Bits (active low)** These signals are driven by the PCI host and they provide command information during the address phase and byte enables during the data phase. **General Purpose I/O** When the CBE2# or the CBE3# interface is not used these can be configured as GPIO 20 and GPIO 21
DEVSEL#	O	H1	PCI	**Device Select (Active Low)** Driven by the MQ-1100/1132 device and, if asserted, indicates that the address is decoded as the target of the current access.
IRDY#	IS	M6	_	**Initiator Ready (active low)** Initiator Ready is driven by the PCI host and indicates the PCI host's ability to complete the current data phase.
TRDY#	O	N8	PCI	**Target Ready (active low)** Target Ready is driven by this chip and indicates the chip's ability to complete the current data phase.

TABLE 2-13: MQ-1132 PCI Bus Interface Pins

Pin Name	Type	MQ-1132 Ball Number	Drive (mA)	Description
STOP#	O	G3	PCI	**Stop Signal (active low)** Driven by the MQ-1100/1132 device. If asserted, it indicates a request to the PCI host to stop the current transaction.
IRL#	OD	P7	_	**Interrupt Request Line (active low)** This is an interrupt request from MQ-1100/1132 device to the PCI host.
PAR	IS/O	P6	PCI	**Parity Signal** This is even parity across AD[31:0] and C/BE[3:0]. It is driven by the PCI host during write accesses and driven by the MQ-1100/1132 device during read accesses.
PERR# (GPIO 24)	IS/O	M11	PCI	**Parity Error (active low)** Driven active by the MQ-1100/1132 device. It is driven active two clocks after a data phase for duration of one clock to indicate parity error on the corresponding data phase. **General Purpose I/O** When the PCI interface is not used this pin can be configured as GPIO 24.
SERR# (GPIO 23)	IS/O	P12	PCI	**System Error (active low)** Driven active by the MQ-1100/1132 device. It is driven active two clocks after an address phase for duration of one clock to indicate parity error on the corresponding address phase. **General Purpose I/O** When the PCI interface is not used this pin can be configured as GPIO 23.
CLKRUN# (GPIO 25)	IS/O	P11	PCI	**Clock Run (active low)** Normally driven low by the PCI host and is an input to the MQ-1100/1132 device. The PCI host drives this signal high for one clock cycle, before tri-stating, to indicate requests by the PCI host/system to stop the PCI clock. If the MQ-1100/1132 device requires the PCI clock, then it responds two clocks after detecting a high state on this pin by driving this signal low for two clock cycles and then tri-stating it. An external weak pull-up resistor is required. **General Purpose I/O** When the PCI interface is not used this pin can be configured as GPIO 25.
BVDD[3:1]	P	P1, M9, M12	_	**Bus Interface Power (3.3 V)**
BGND[3:1]	G	M1, N9, L14	_	**Bus Interface Ground**

TABLE 2-14: MQ-1100/1132 FPI Pins

Pin Name	Type	MQ-1100 Pin Number	MQ-1100 Ball Number	MQ-1132 Ball Number	Drive (mA)	Description
ENVDD (GPIO)	IS/O	11	E2	G2	8	**Enable V_{DD}** In panel power-up sequence, ENVDD is asserted first. In panel power-down sequence, ENVDD is de-asserted last. If not used as ENVDD, you can configure ENVDD as ENCTL, which is activated one frame after the data and control signals are activated and deactivated one frame before data and control signals are deactivated. After reset, this pin is driven low. **General Purpose I/O** If not used as ENVDD or ENCTL, this can be configured as a GPIO pin.
ENVEE (GPIO)	IS/O	12	F2	G1	8	**Enable V_{EE}** In panel power-up sequencing, ENVEE is asserted last. In panel power-down sequencing, ENVEE is de-asserted first. If not used as ENVEE, this signal can be configured as ENCTL, which is activated one frame after data and control signals are activated and deactivated one frame before data and control signals are deactivated. After reset, ENVEE is driven low. **General Purpose I/O** If not used as ENVEE or ENCTL, this can be configured as a GPIO pin.
FD[23:18] FD[15:10] FD[7:2] (GPIO)	IS/O	74,75, 76, 77, 78, 79, 80,81, 83, 85, 86, 87, 89, 91,92, 93, 94, 95	A9, A8, B9, B8, C7, C6, B7, C5, A6, C4, C3, C2, B5, B4, B3, A5, A4, A3	C14, A14, A13, B12, B11,C11, B10, A10, B9, C9,B8, A8, C7, B7, A6, B6, C6, A5	8	**Flat Panel Data (programmable polarity)** Provide data to the flat panel. Active approximately one frame before ENCTL is asserted and deactivated approximately one frame after ENCTL is de-asserted. Driven low during reset as well as when the flat panel is disabled, regardless of its polarity. **General Purpose I/O** If not used to drive the flat panel, these pins can be configured as GPIO pins.
FSCLK (GPIO)	IS/O	7	D1	E3	16	**Flat Panel Shift Clock (programmable polarity)** For active high FSCLK, the rising edge of this clock outputs the flat panel data and control signals, and the falling edge of this clock externally latches the flat panel data and control signals. For active low FSCLK, the falling edge of this clock outputs flat panel data and control signals, and the rising edge of this clock externally latches flat panel data and control signals. FSCLK is driven low during reset and when the flat panel is disabled regardless of its polarity. **General Purpose I/O** If not used as ENVEE or ENCTL, this can be configured as a GPIO pin.

TABLE 2-14: MQ-1100/1132 FPI Pins

Pin Name	Type	MQ-1100 Pin Number	MQ-1100 Ball Number	MQ-1132 Ball Number	Drive (mA)	Description
FDE FSSP (GPIO)	IS/O	3	A1	D2	8	**Flat Panel Data Enable (programmable polarity)** Indicates valid data area. Timing is the same as flat panel data. Normally used for TFT LCD. This signal is driven low during reset and when the flat panel is disabled, regardless of its polarity. **Flat Panel Source Driver Start Pulse (programmable polarity)** Outputs the start pulse for source (column) driver which occurs one shift clock before the first data of each line. This can be used for driving the TFT panel directly. **General Purpose I/O** If not used as FDE or FSSP, this pin can be configured as a GPIO pin.
FHSYNC FLP (GPIO)	IS/O	10	E1	F3	8	**Flat Panel Horizontal Sync for TFT LCD (programmable polarity)** Horizontal sync for TFT LCD panels. Driven low during reset and when the flat panel is disabled regardless of its polarity. **Flat panel LP for TFT LCD panels (programmable polarity)** Outputs LP for driving TFT panels directly, which is generated four clocks from the falling edge of the internal HSYNC for a duration of either one or two clocks. LP for TFT/STN LCD panels (programmable polarity) Line Pulse for STN LCD panels. **General Purpose I/O** If not used as FHSYNC or FLP, this pin can be configured as a GPIO pin.
FVSYNC FGSP FLM (GPIO)	IS/O	9	F1	F1	4	**Flat Panel Vertical Syncronization for TFT LCD (programmable polarity)** Vertical sync for TFT LCD panels. Drives low during reset and when the flat panel is disabled (regardless of its polarity) **Flat panel gate Driver Start Pulse (programmable polarity)** Configureable to the output start pulse for gate (row) driver: to drive TFT panels directly **FLM for STN LCD panels (programmable polarity)** Configureable as the First Line marker for STN LCD panels. **General Purpose I/O** If not used as a FVSYNC, FGSP, or FLM, this pin can be configured as a GPIO pin.
FMOD (GPIO)	IS/O	5	B2	E2	4	**Modulation clock (programmable polarity)** Can be driven to toggle every frame or every programmable number of lines. FMOD is required when driving a TFT panel directly or for some STN panels. During reset, this signal is tri-stated together with a weak pull-down enabled. **General Purpose I/O** If not used as FMOD, this pin can be configured as a GPIO pin.

TABLE 2-14: MQ-1100/1132 FPI Pins

Pin Name	Type	MQ-1100 Pin Number	MQ-1100 Ball Number	MQ-1132 Ball Number	Drive (mA)	Description
FLCLK (GPIO)	IS/O	4	B1	D3	4	**Flat Panel Line Clock (programmable polarity)** This clock pulse occurs once per line as defined in GC0BR and can be used as a clock for the gate (row) driver. During reset, FLCLK is tri-stated together with a weak internal pull-down enabled. **General Purpose I/O** If not used as FLCLK, this pin can be configured as a GPIO pin.
PWM0 (GPIO)	IS/O	2	E3	C2	8	**Pulse Width Modulation 0 (PWM, programmable polarity)** This pulse width modulation clock is enabled just before flat panel control or data is enabled and deactivated just after flat panel control or data is disabled. This pulse can control the external contrast/brightness logic or backlight. During reset, PWM0 is tri-stated together with a weak internal pull-down resistor enabled. **General Purpose I/O** If not used as PWM0, this pin can be configured as GPIO pin.
PWM1 FLCLKA (GPIO)	IS/O	1	D2	B1	8	**Pulse Width Modulation 1 (programmable polarity)** This pulse width modulation clock is enabled just before the flat panel control or data is enabled and deactivated just after the flat panel control or data is disabled. This pulse can control the external contrast/brightness logic or backlight. During reset, this signal is tri-stated together with a weak internal pull-down resistor enabled. **Flat Panel Line Clock Alternate (programmable polarity)** This pin can be configured to output the line clock. **General Purpose I/O** If not used as PWM1 or FLCLKA, this pin can be configured as a GPIO pin.
FVDD[2:1]	P	84, 8	A7, C1	A9, F2	_	**Flat Panel Power (3.3 V)**
FGND[2:1]	G	82, 6	D6, E5	C10, E1	_	**Flat Panel Ground**

TABLE 2-15: Additional MQ-1132 FPI Pins

Pin Name	Type	MQ-1132 Ball Number	Drive (mA)	Description
FVDD[3]	P	B4	_	**Flat Panel Power (3.3 V)**
FGND[3]	G	C5	_	**Flat Panel Ground**

TABLE 2-16: MQ-1132 USB Interface Pins

Pin Name	Type	MQ-1100 Pin Number	MQ-1100 Ball Number	MQ-1132 Ball Number	Drive (mA)	Description
PVDD	AP	68	D10	F14	_	**Port 1 Power (3.3 V)** USB function/host power.
PGND	AG	67	B10	G13	_	**Port 1 Ground** USB function/host ground.
P1DP	A	66	D8	G14	_	**Port 1 Positive Data** USB function positive data. Requires an external 1.5k ohm pull-up resistor.
P1DN	A	65	D9	G12	_	**Port 1 Negative Data** USB function negative data.

TABLE 2-17: MQ-1132 Additional USB Host Interface Pins

Pin Name	Type	MQ-1132 Ball Number	Drive (mA)	Description
P2DP	A	F12	_	**Port 2 Positive Data** USB host positive data.
P2DN	A	F13	_	**Port 2 Negative Data** USB host negative data.

TABLE 2-18: MQ-1132 I^2C Codec Interface Pins [1]

Pin Name	Type	MQ-1132 Ball Number	Drive (mA)	Description
SRCLK (GPIO 40)	IS/O	D1	4	**Serial Root Clock Input** Can be used to supply the root clock for the Codec interface for all modes of operation. **General Purpose I/O** If this pin is not used as SRCLK, it can be configured as a GPIO 40. Upon reset, this pin tri-stated and its input buffer is disabled.
SMCLK (GPIO 41)	IS/O	C3	4	**Serial Master Clock Output** Can be used to output the master clock to the external Codec for all modes of operation. **General Purpose I/O** If this pin is not used as SMCLK, it can be configured as GPIO 41. Upon reset, this pin tri-stated and its input buffer is disabled.

TABLE 2-18: MQ-1132 I²C Codec Interface Pins [1]

Pin Name	Type	MQ-1132 Ball Number	Drive (mA)	Description
SCLK (GPIO 42)	IS/O	C1	4	**Serial Bit Clock** Input in modes 0 and 2 and an output in modes 1 and 3. **General Purpose I/O** If this pin is not used as SCLK, it can be configured as GPIO 42. Upon reset, this is pin tri-stated and its input buffer is disabled.
FSYNC (GPIO 43)	IS/O	B2	4	**Frame Synchronization** Input in modes 0 and 1 and an output in modes 2 and 3. **General Purpose I/O** If this pin is not used as FSYNC, it can be configured as GPIO 43. Upon reset, this pin is tri-stated and its input buffer is disabled.
SIN (GPIO 44)	IS/O	A2	4	**Serial Data Input** Serial input data **General Purpose I/O** If this pin is not used as SIN, it can be configured as GPIO 44. Upon reset, this pin is tri-stated and its input buffer is disabled.
SOUT (GPIO 45)	IS/O	B3	4	**Serial Data Output** Serial output data **General Purpose I/O** If this pin is not used as SOUT, it can be configured as GPIO 45. Upon reset, this pin is tri-stated and its input buffer is disabled.

1. These pins share power and ground with the FPI.

TABLE 2-19: MQ-1132 LED, SPI, and GPIO Pins [1]

Pin Name	Type	MQ-1132 Ball Number	Drive (mA)	Description
SS# (GPIO 50)	IS/O	N4	4	**Slave Select** In SPI master mode, this pin can be optionally used to indicate multiple-master bus contention in which case this pin becomes an input. In SPI master mode with mode fault detection disabled, this pin can be optionally used to generate Slave Select signal that toggles for every data transfer in CPHA=0 type of transfer format. **General Purpose I/O** If not used as SS# this pin can be used as GPIO 50. Upon reset, this pin is tri-stated with weak pull-up enabled and its input buffer disabled.
SCK SPSCLK (GPIO 51)	IS/O	N3	4	**SPI Data Transfer Clock** Can be used as an SPI Clock Line output. **General Purpose I/O** If not used as SS# this pin can be used as GPIO 51. Upon reset, this pin is tri-stated with weak pull-up enabled and its input buffer disabled.

TABLE 2-19: MQ-1132 LED, SPI, and GPIO Pins [1]

Pin Name	Type	MQ-1132 Ball Number	Drive (mA)	Description
MOSI (GPIO 52)	IS/O	L3	4	**SPI Master Out/Slave In** Can be used as an output data in the SPI master mode or as an input data in the SPI slave mode. **General Purpose I/O** If not used as SS# this pin can be used as GPIO 52. Upon reset, this pin is tri-stated with weak pull-up enabled and its input buffer disabled.
MISO (GPIO 53)	IS/O	L1	4	**SPI Master In/Slave Out** Can be used to input data in SPI master mode or to output data in SPI slave mode. **General Purpose I/O** If not used as SS# this pin can be used as GPIO 53. Upon reset, this pin is tri-stated with weak pull-up enabled and its input buffer disabled.
LED (GPIO 54)	IS/O	H14	4	**LED output** Can be used as a programmable LED output. **General Purpose I/O** If not used as SS# this pin can be used as GPIO 54. Upon reset, this pin is tri-stated and its input buffer disabled.
GPIO55	IS/O	H12	4	**General Purpose I/O** Upon reset, this pin is tri-stated and its input buffer is disabled.

1. These pins share power and ground with the CPU pins.

TABLE 2-20: MQ-1132 GPIO Pins [1]

Pin Name	Type	MQ-1132 Ball Number	Drive (mA)	Description
GPIO60	IS/O	D13	4	**General Purpose I/O** These pins can be used as GPIO pins. Upon reset, both output buffer and input buffer are disabled.
GPIO61		C13		
GPIO62		B14		
GPIO63		B13		
GPIO64		A12		
GPIO65		C12		
GPIO66		A11		

1. These pins share power and ground with the FPI.

TABLE 2-21: CPU Mode Pin Settings

Pins [1]				CPU Mode
MD[1:0]	BS#	CKIO	PCIMD#	
XX	X	X	0	**PCI bus version 2.1 (Only for the MQ-1132)**
10	X	X	1	**Hitachi SH3**
11	X	X	1	**Hitachi SH4**
01	0	X	1	**NEC VR-4111, VR-4121**
01	1	X	1	**Intel SA-1110/SA-2**
00	0	X	1	**Reserved**
00	1	1	1	**Motorola DragonBall**
00	1	0	1	**NAND chain test mode**

1. An X represents a “Don’t care” bit. The MD[1:0], BS#, CKIO, and PCIMD# pins determine which CPU is interfacing with the MQ-1132. Bit settings for these pins relative to different CPU modes is specified in Table 2-21.

Table 2-22 specifies the 100-pin TQFP and 132-pin BGA pin order and assignments.

TABLE 2-22: MQ-1100/1132 Pin Order and Assignments

Package			Interface				
100-Pin TQFP	**100-Pin BGA**	**132-Pin BGA**	**Hitachi SH-7709 SH-7750**	**NEC VR-4111 VR-4121**	**Intel SA-1110 XScale**	**Motorola DragonBall**	**PCI Version 2.1**
1	D2	B1	PWM1	PWM1	PWM1	PWM1	PWM1
2	E3	C2	PWM0	PWM0	PWM0	PWM0	PWM0
3	A1	D2	FDE	FDE	FDE	FDE	FDE
4	B1	D3	FLCLK	FLCLK	FLCLK	FLCLK	FLCLK
5	B2	E2	FMOD	FMOD	FMOD	FMOD	FMOD
6	E5	E1	FGND1	FGND1	FGND1	FGND1	FGND1
7	D1	E3	FSCLK	FSCLK	FSCLK	FSCLK	FSCLK
8	C1	F2	FVDD1	FVDD1	FVDD1	FVDD1	FVDD1
9	F1	F1	FVSYNC	FVSYNC	FVSYNC	FVSYNC	FVSYNC
10	E1	F3	FHSYNC	FHSYNC	FHSYNC	FHSYNC	FHSYNC
11	E2	G2	ENVDD	ENVDD	ENVDD	ENVDD	ENVDD
12	F2	G1	ENVEE	ENVEE	ENVEE	ENVEE	ENVEE
13	G2	G3	A18	A18	A18	A18	STOP#
14	E6	H3	CGND3	CGND3	CGND3	CGND3	CGND3
15	H2	H1	A17	A17	A17	A17	DEVSEL#
16	G1	H2	CVDD3	CVDD3	CVDD3	CVDD3	CVDD3
17	H1	J1	A16	A16	A16	A16	AD31
18	J2	J2	A15	A15	A15	A15	AD30
19	J1	J3	A14	A14	A14	A14	AD29

TABLE 2-22: MQ-1100/1132 Pin Order and Assignments

Package			Interface				
100-Pin TQFP	100-Pin BGA	132-Pin BGA	Hitachi SH-7709 SH-7750	NEC VR-4111 VR-4121	Intel SA-1110 XScale	Motorola DragonBall	PCI Version 2.1
20	J3	K1	A13	A13	A13	A13	AD28
21	K1	K2	A12	A12	A12	A12	AD27
22	H3	K3	A11	A11	A11	A11	AD26
23	G3	L2	A10	A10	A10	A10	AD25
24	H4	M2	A9	A9	A9	A9	AD24
25	J4	N1	A8	A8	A8	A8	AD23
26	K2	N2	A7	A7	A7	A7	AD22
27	K3	P3	A6	A6	A6	A6	AD21
28	G4	M3	A5	A5	A5	A5	AD20
29	J5	P4	A4	A4	A4	A4	AD19
30	H5	M4	A3	A3	A3	A3	AD18
31	G5	N5	A2	A2	A2	A2	AD17
32	F3	P5	A1	A1	A1	A1	AD16
33	K5	N6	CS#	CS#	CS#	CS#	FRAME#
34	K6	P6	BS#	mode/GPIO7	mode/GPIO7	mode/GPIO7	PAR
35	J6	M6	RD/ WR#	RD#	OE#	OE#	IRDY#
36	F6	N7	CGND2	CGND2	CGND2	CGND2	CGND2
37	H6	P7	IRL#	IRL#	IRL#	IRL#	IRL#
38	K4	M7	CVDD2	CVDD2	CVDD2	CVDD2	CVDD2
39	J7	M8	D15	D15	D15	D15	AD15
40	J8	P8	D14	D14	D14	D14	AD14
41	K8	N8	RDY#	RDY	RDY	DTACK#	TRDY#
42	K9	P9	CKIO	WR#	WR#	GPIO6	CLK
43	F5	N9	BGND2	BGND2	BGND2	BGND2	BGND2
44	K7	M9	BVDD2	BVDD2	BVDD2	BVDD2	BVDD2
45	J9	P10	D13	D13	D13	D13	AD13
46	H7	N10	D12	D12	D12	D12	AD12
47	H8	M10	D11	D11	D11	D11	AD11
48	H9	N11	D10	D10	D10	D10	AD10
49	G6	N12	D9	D9	D9	D9	AD9
50	G7	P13	D8	D8	D8	D8	AD8
51	E9	N13	WE1#	BE1#	BE1#	UWE#	C/BE1#
52	G8	M14	D7	D7	D7	D7	AD7
53	G9	M13	D6	D6	D6	D6	AD6

TABLE 2-22: MQ-1100/1132 Pin Order and Assignments

Package			Interface				
100-Pin TQFP	**100-Pin BGA**	**132-Pin BGA**	**Hitachi SH-7709 SH-7750**	**NEC VR-4111 VR-4121**	**Intel SA-1110 XScale**	**Motorola DragonBall**	**PCI Version 2.1**
54	K10	M12	BVDD1	BVDD1	BVDD1	BVDD1	BVDD1
55	J10	L13	D5	D5	D5	D5	AD5
56	E7	L14	BGND1	BGND1	BGND1	BGND1	BGND1
57	E8	L12	D4	D4	D4	D4	AD4
58	F7	K13	D3	D3	D3	D3	AD3
59	F8	K14	D2	D2	D2	D2	AD2
60	F9	K12	D1	D1	D1	D1	AD1
61	H10	J13	D0	D0	D0	D0	AD0
62	D7	J14	CGND1	CGND1	CGND1	CGND1	CGND1
63	C9	J12	WE0#	BE0#	BE0#	LWE#	C/BE0#
64	G10	H13	CVDD1	CVDD1	CVDD1	CVDD1	CVDD1
65	D9	G12	P1DN(Dev)	P1DN(Dev)	P1DN(Dev)	P1DN(Dev)	P1DN(Dev)
66	D8	G14	P1DP(Dev)	P1DP(Dev)	P1DP(Dev)	P1DP(Dev)	P1DP(Dev)
67	B10	G13	PGND	PGND	PGND	PGND	PGND
68	D10	F14	PVDD	PVDD	PVDD	PVDD	PVDD
69	C10	E14	AVDDO	AVDDO	AVDDO	AVDDO	AVDDO
70	F10	E13	OSCFI	OSCFI	OSCFI	OSCFI	OSCFI
71	E10	E12	OSCFO	OSCFO	OSCFO	OSCFO	OSCFO
72	A10	D14	AGNDO	AGNDO	AGNDO	AGNDO	AGNDO
73	C8	D12	POR#	POR#	POR#	POR#	POR#
74	A9	C14	FD23	FD23	FD23	FD23	FD23
75	A8	A14	FD22	FD22	FD22	FD22	FD22
76	B9	A13	FD21	FD21	FD21	FD21	FD21
77	B8	B12	FD20	FD20	FD20	FD20	FD20
78	C7	B11	FD19	FD19	FD19	FD19	FD19
79	C6	C11	FD18	FD18	FD18	FD18	FD18
80	B7	B10	FD15	FD15	FD15	FD15	FD15
81	C5	A10	FD14	FD14	FD14	FD14	FD14
82	D6	C10	FGND2	FGND2	FGND2	FGND2	FGND2
83	A6	B9	FD13	FD13	FD13	FD13	FD13
84	A7	A9	FVDD2	FVDD2	FVDD2	FVDD2	FVDD2
85	C4	C9	FD12	FD12	FD12	FD12	FD12
86	C3	B8	FD11	FD11	FD11	FD11	FD11
87	C2	A8	FD10	FD10	FD10	FD10	FD10

TABLE 2-22: MQ-1100/1132 Pin Order and Assignments

Package			Interface				
100-Pin TQFP	100-Pin BGA	132-Pin BGA	Hitachi SH-7709 SH-7750	NEC VR-4111 VR-4121	Intel SA-1110 XScale	Motorola DragonBall	PCI Version 2.1
88	D5	C8	CGND4	CGND4	CGND4	CGND4	CGND4
89	B5	C7	FD7	FD7	FD7	FD7	FD7
90	A2	A7	CVDD4	CVDD4	CVDD4	CVDD4	CVDD4
91	B4	B7	FD6	FD6	FD6	FD6	FD6
92	B3	A6	FD5	FD5	FD5	FD5	FD5
93	A5	B6	FD4	FD4	FD4	FD4	FD4
94	A4	C6	FD3	FD3	FD3	FD3	FD3
95	A3	A5	FD2	FD2	FD2	FD2	FD2
96	F4	B5	PDWN#/GPIO4	PDWN#/GPIO4	PDWN#/GPIO4	PDWN#/GPIO4	PDWN#/GPIO4
97	E4	A4	MD3/GPIO3	MD3/GPIO3	MD3/GPIO3	MD3/GPIO3	MD3/GPIO3
98	B6	C4	MD2/GPIO2	MD2/GPIO2	MD2/GPIO2	MD2/GPIO2	MD2/GPIO2
99	D4	A3	MD1/GPIO1	MD1/GPIO1	MD1/GPIO1	MD1/GPIO1	MD1/GPIO1
100	D3	A1	MD0/GPIO0	MD0/GPIO0	MD0/GPIO0	MD0/GPIO0	MD0/GPIO0
		A2	SIN/GPIO44	SIN/GPIO44	SIN/GPIO44	SIN/GPIO44	SIN/GPIO44
		A11	GPIO66	GPIO66	GPIO66	GPIO66	GPIO66
		A12	GPIO64	GPIO64	GPIO64	GPIO64	GPIO64
		B2	FSYNC/GPIO43	FSYNC/GPIO43	FSYNC/GPIO43	FSYNC/GPIO43	FSYNC/GPIO43
		B3	SOUT/GPIO45	SOUT/GPIO45	SOUT/GPIO45	SOUT/GPIO45	SOUT/GPIO45
		B4	FVDD3	FVDD3	FVDD3	FVDD3	FVDD3
		B13	GPIO63	GPIO63	GPIO63	GPIO63	GPIO63
		B14	GPIO62	GPIO62	GPIO62	GPIO62	GPIO62
		C1	SCLK/GPIO42	SCLK/GPIO42	SCLK/GPIO42	SCLK//GPIO42	SCLK/GPIO42
		C3	SMCLK/GPIO41	SMCLK/GPIO41	SMCLK/GPIO41	SMCLK/GPIO41	SMCLK/GPIO41
		C5	FGND3	FGND3	FGND3	FGND3	FGND3
		C12	GPIO65	GPIO65	GPIO65	GPIO65	GPIO65
		C13	GPIO61	GPIO61	GPIO61	GPIO61	GPIO61
		D1	SRCLK/GPIO40	SRCLK/GPIO40	SRCLK/GPIO40	SRCLK/GPIO40	SRCLK/GPIO40
		D13	GPIO60	GPIO60	GPIO60	GPIO60	GPIO60
		F12	P2DP(Host)	P2DP(Host)	P2DP(Host)	P2DP(Host)	P2DP(Host)
		F13	P2DN(Host)	P2DN(Host)	P2DN(Host)	P2DN(Host)	P2DN(Host)
		H12	GPIO55	GPIO55	GPIO55	GPIO55	GPIO55
		H14	LED/GPIO54	LED/GPIO54	LED/GPIO54	LED/GPIO54	LED/GPIO54
		L1	MISO/GPIO53	MISO/GPIO53	MISO/GPIO53	MISO/GPIO53	MISO/GPIO53
		L3	MOSI/GPIO52	MOSI/GPIO52	MOSI/GPIO52	MOSI/GPIO52	MOSI/GPIO52

TABLE 2-22: MQ-1100/1132 Pin Order and Assignments

Package			Interface				
100-Pin TQFP	**100-Pin BGA**	**132-Pin BGA**	**Hitachi SH-7709 SH-7750**	**NEC VR-4111 VR-4121**	**Intel SA-1110 XScale**	**Motorola DragonBall**	**PCI Version 2.1**
		M1	BGND3	BGND3	BGND3	BGND3	BGND3
		M5	GPIO20	GPIO20	GPIO20	GPIO20	C/BE2#
		M11	GPIO24	GPIO24	GPIO24	GPIO24	PERR#
		N3	SCK/GPIO51	SCK/GPIO51	SCK/GPIO51	SCK/GPIO51	SCK/GPIO51
		N4	SS#/GPIO50	SS#/GPIO50	SS#/GPIO50	SS#/GPIO50	SS#/GPIO50
		N14	PCIMD#/GPIO5	PCIMD#/GPIO5	PCIMD#/GPIO5	PCIMD#/GPIO5	PCIMD#/GPIO5
		P1	BVDD3	BVDD3	BVDD3	BVDD3	BVDD3
		P2	GPIO21	GPIO21	GPIO21	GPIO21	C/BE3#
		P11	GPIO25	GPIO25	GPIO25	GPIO25	CLKRUN#
		P12	GPIO23	GPIO23	GPIO23	GPIO23	SERR#
		P14	GPIO22	GPIO22	GPIO22	GPIO22	IDSEL

2.3 Package Descriptions

The MQ-1100/1132, LCD and Peripheral Controller is offered in three package designs: a 100-pin MQ-1100 TQFP package; a 100-pin MQ-1100 BGA package; and the MQ-1132 132-pin BGA package. *Figure 2-1* on page 33 through *Figure 2-7* on page 37 show the package designs for MQ-1100 and MQ-1132.

2.3.1. MQ-1100 BGA Package Designs

This section illustrates three different perspectives for the MQ-1100 BGA package: the top, the bottom and the side.

The following three figures specify the MQ-1100 BGA package: top view, bottom view, and side view.

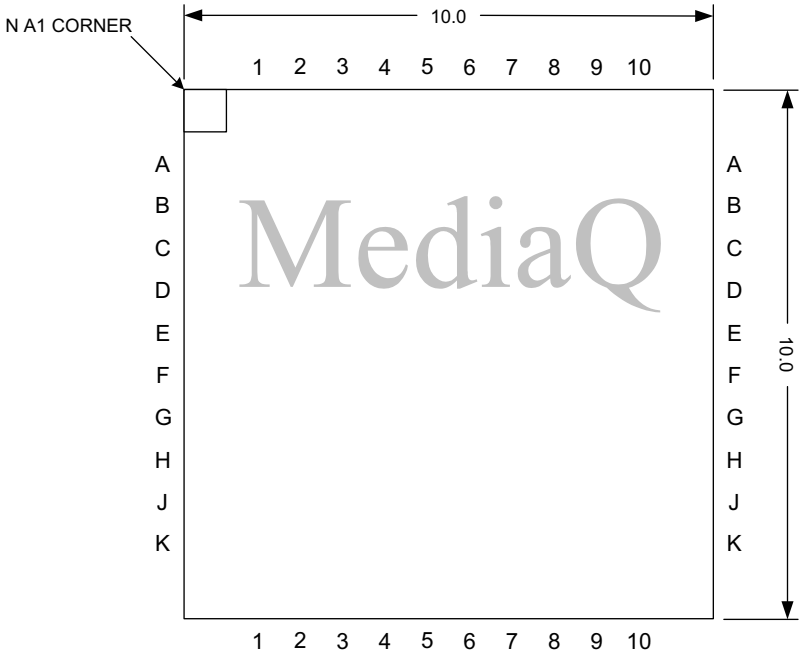


Figure 2-1 MQ-1100 – BGA Package Top View with Dimensions in Millimeters

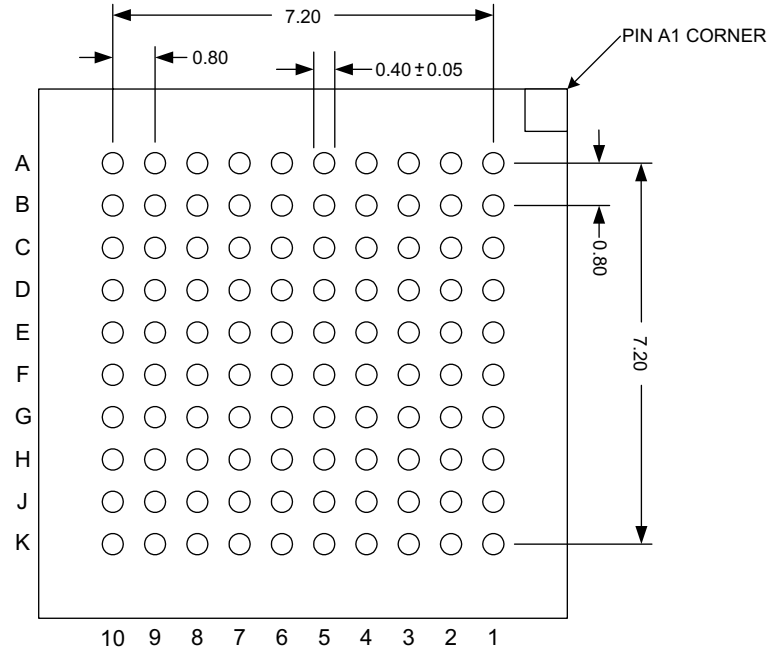


Figure 2-2 MQ-1100 BGA Package - Bottom View with Dimensions in Millimeters

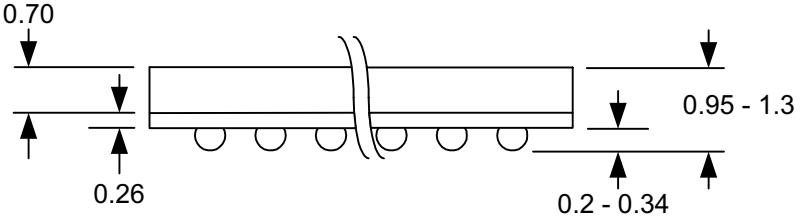


Figure 2-3 MQ-1100 BGA Package – Side View with Dimensions in Millimeters

2.3.2. MQ-1100 TQFP Package Designs

The MQ-1100 offered as a TQFP package is illustrated in *Figure 2-4* on page 35 and *Figure 2-5* on page 36.

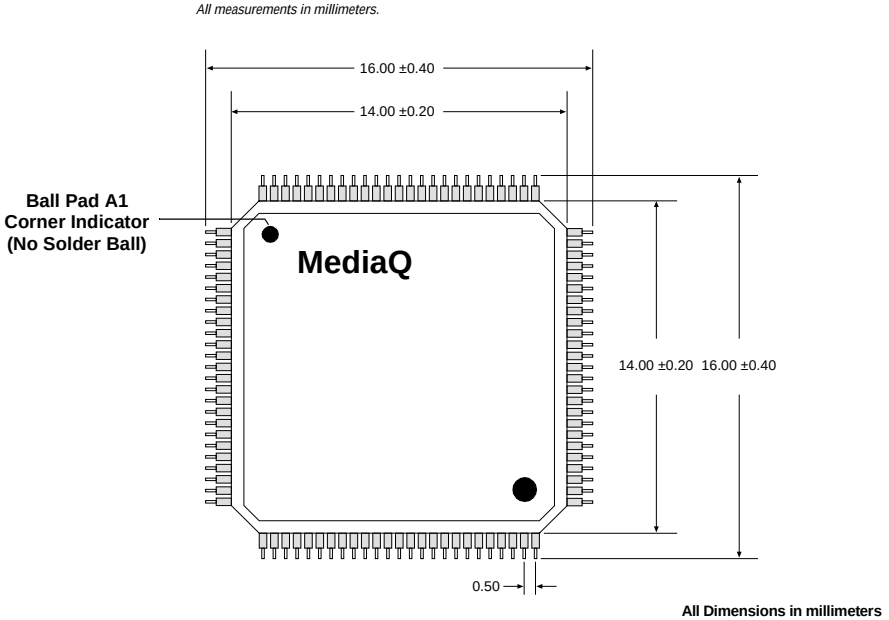
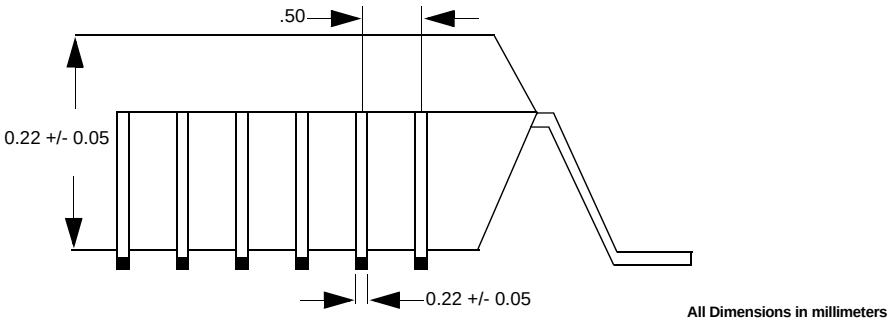


Figure 2-4 MQ-1100 TQFP – Dimensions and Package Top View



MQ-1100 TQFP Package – Side View

2.3.3. MQ-1132 BGA Package Designs

The MQ-1132 LCD and Peripheral Controller is exclusively offered as a BGA package. *Figure 2-5* on page 36 through *Figure 2-7* on page 37, illustrate the top, bottom and side views of the this package.

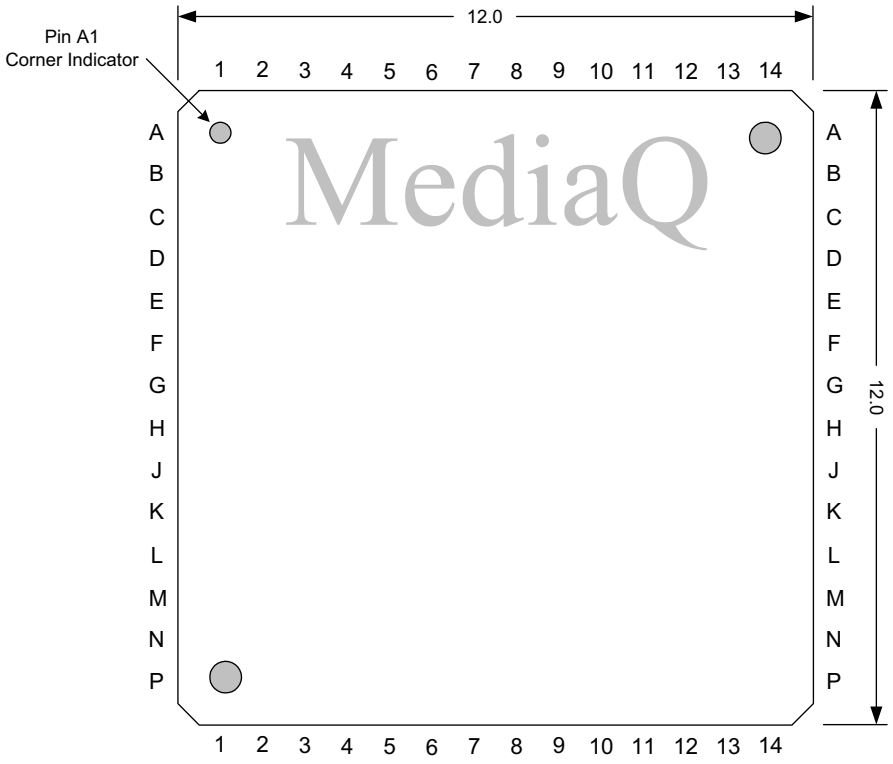


Figure 2-5 MQ-1132 BGA Package Top View with Dimensions in Millimeters

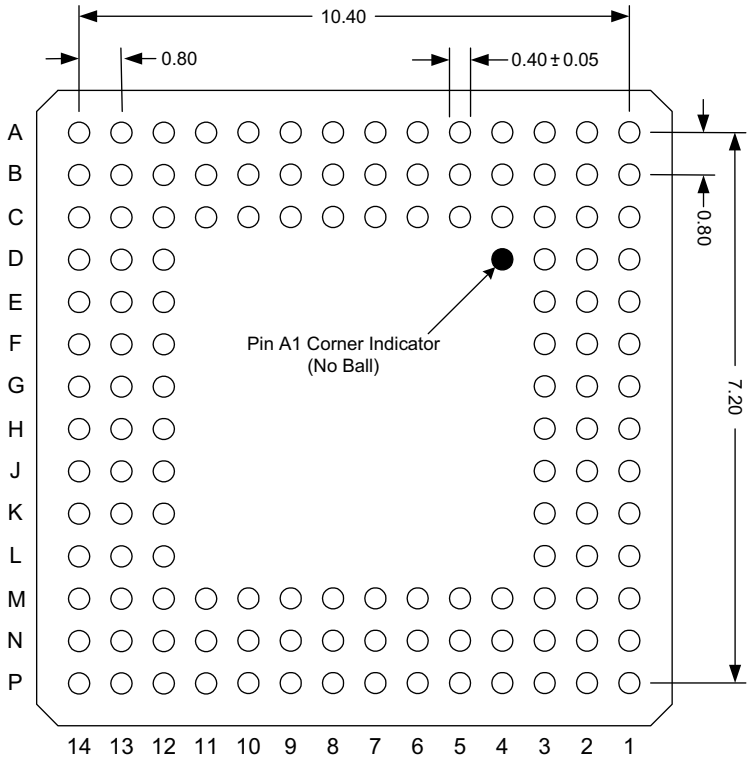


Figure 2-6 MQ-1132 BGA Package – Bottom View with Dimensions in Millimeters

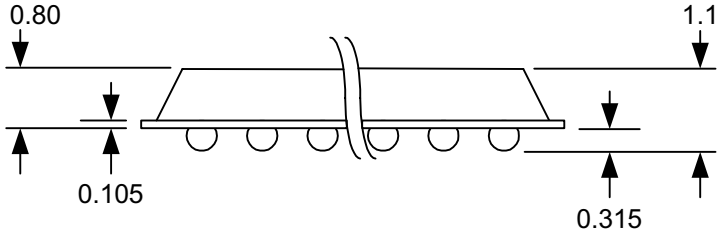


Figure 2-7 MQ-1132 BGA Package – Side View with Dimensions in Millimeters

2.4 Part Numbering

Part numbers are printed on the top of each device package. The top of each device (MQ-1100 and MQ-1132) is marked as illustrated in *Figure 2-8* on page 38. The illustration specifies each character of the part number.

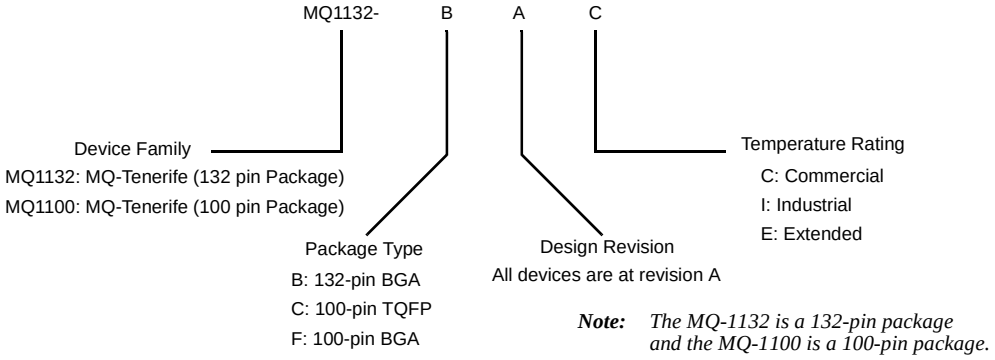


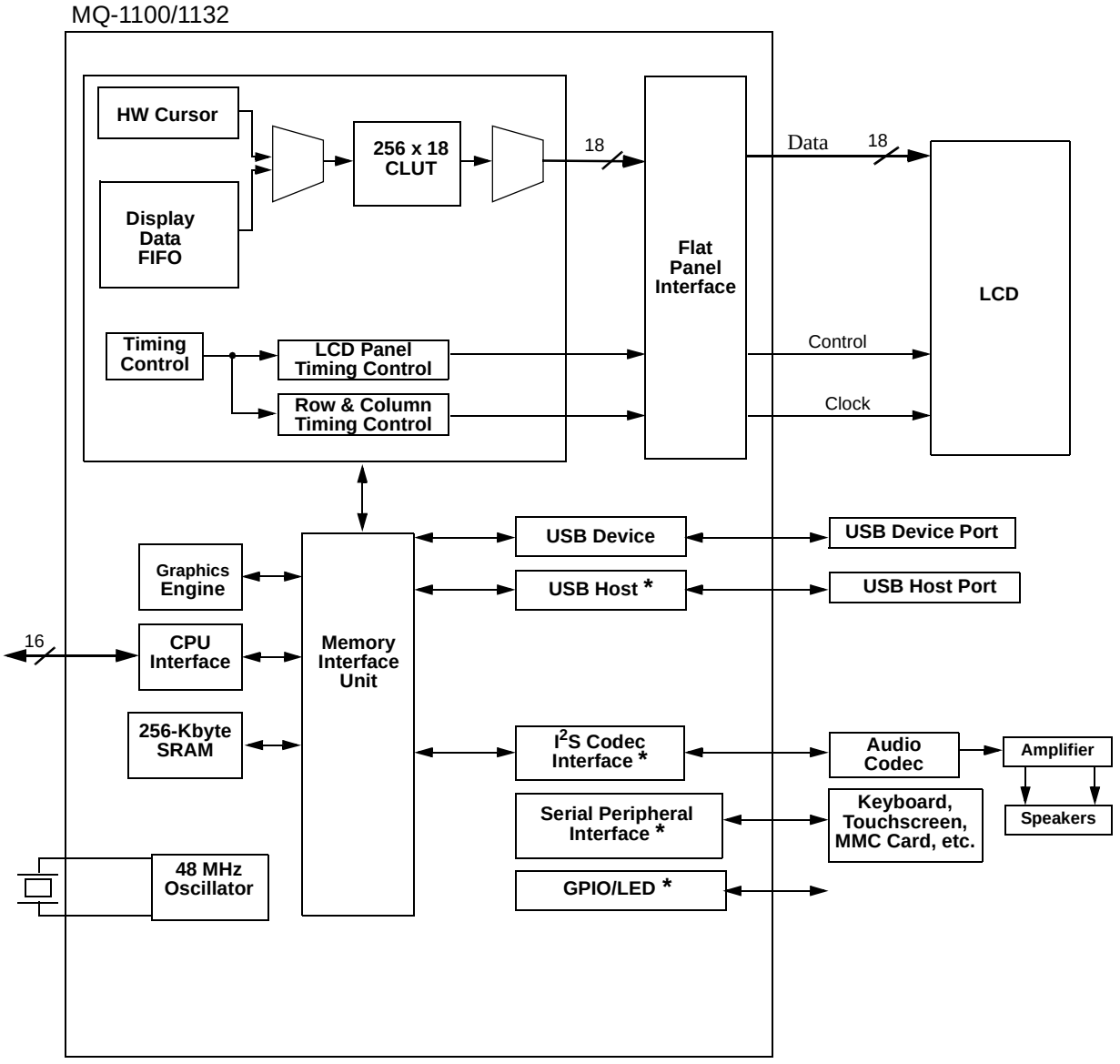
Figure 2-8 Part Number Definition

Chapter 3

3-1. FUNCTIONAL DESCRIPTION

The main functional components of the MQ-1100/MQ-1132 device are (see *Figure 3-1*):

- CPU Interface
- Interrupt Controller
- USB host controller - MQ-1132 only
- USB function
- Serial Peripheral Interface (SPI) - MQ-1132 only
- I2S Codec Interface(I^2S) - MQ-1132
- Graphics Engine
- On-chip Memory Interface Unit (MIU)
- Graphics Controller
- Flat Panel Interface (FPI)



Note: *"*"These connections are only available with the MQ-1132 device.*

Figure 3-1 MQ-1100/1132 Block Diagram

3.2 CPU Interface

Figure 3-2, "MQ-1132 CPU Interface," on page 41, illustrates the CPU interface architecture and how the different modules interact. Depending on the type of operation, the CPU interface can read or write directly into the on-chip memory or, in the case of a graphical operation, the CPU interface can use the graphics engine to store image data in memory. Image data can come from the system memory or through a series of graphics operations (such as the area fill, block move, line draw, etc.).

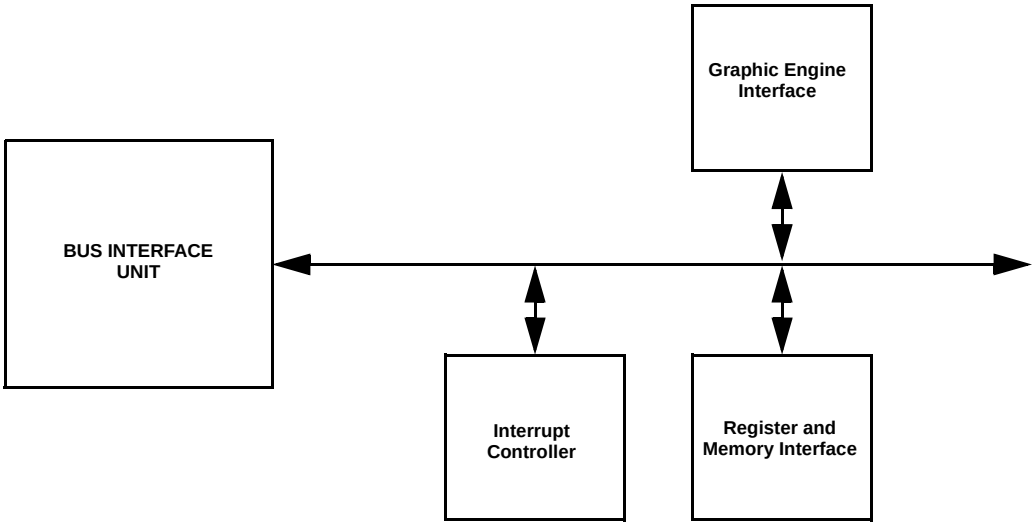


Figure 3-2 MQ-1132 CPU Interface

3.2.1. PCI Bus interface

The MQ-1132 controller supports the PCI Version 2.1 bus configuration by acting as a target device, supporting 32-bit memory and I/O operations and byte lane swapping: there is full 32-bit address decoding available with the PCI. The 1132 controller achieves read/write burst cycles with burst access. No external buffers are required when interfacing to the MQ-1132 controller to the PCI bus. In order to support Mobile PCI version 1.0, an additional PCI signal has been added. CLKRUN# is used to control the PCI clock. For more information about CLKRUN#, see the Mobile PCI version 1.0 documentation. If the feature is not used, the CLKRUN# pin should be pulled up externally.

3.3 Interrupt Controller

The integrated interrupt controller in the MQ-1100/1132 has 15 programmable interrupt sources, each of which can be optionally masked (disabled). A global interrupt enable bit is provided. All interrupt sources include:

- Interrupts from graphics controller.
  - Vertical synchronization – rising edge.
  - Vertical synchronization – falling edge.
  - Vertical display enable – rising edge.
  - Vertical display enable – falling edge.
- Interrupts from graphics engine.
  - Command FIFO half empty.
  - Command FIFO empty.
  - Source FIFO half empty.
  - Source FIFO empty.
  - Graphics engine is idle.
- Interrupts from general-purpose I/O port
  - Input from GPIO 0; low-level or high-level input can be programmed to generate interrupt.
  - Input from GPIO 1, low-level or high-level input can be programmed to generate interrupt.
  - Input from GPIO 2, low-level or high-level input can be programmed to generate interrupt.
- Interrupt from the BIU, CPU bus cycle abort.
- Interrupt from the USB device, USB device wake-up interrupt
- Interrupt from the USB host (MQ-1132 only).
  - USB host controller OHCI compatible interrupts.
  - USB host remote wake-up in low power state when oscillator is disabled.
  - USB host controller global suspend mode interrupt.
- Interrupt from SPI interface (MQ-1132 only).
- Interrupt from I^2S codec interface (MQ-1132 only).

When an enabled-interrupt condition is detected, the corresponding bit in the interrupt status register is set. The MQ-1132 asserts the IRL# output pin to signal the CPU if the global interrupt enable bit is enabled. When the CPU responds to the interrupt, the interrupt handler reads the status register to determine the cause of the interrupt. The interrupt handler must then explicitly clear the interrupt by writing a 1 to the corresponding bit in the interrupt status register or associated peripheral interrupt status register (see description in the Interrupt Controller section of the Programming chapter). All status bits except for those coming from SPI, I^2S, or USB are “sticky,” they are set when the interrupt condition is detected and remain set until explicitly cleared. The active level of the IRL# output is programmable.

If the global-enable bit is disabled, then the CPU checks the interrupt by polling the interrupt status register. A status register reports which interrupts have been detected. A second status register containing the “raw” interrupt status is available. Instead of waiting for the IRL# signal, the driver software may choose to poll this “raw” interrupt status register until the interrupt condition is seen. For this type of interrupt scheme, the sources to be polled should be masked off.

When using GPIO pins as interrupt sources, first configure each of the pins as an input by programming the GPIO control registers. The GPIO interrupt flags are level-triggered. If the GPIO pin is programmed as active high, the high level will set the interrupt; if it is programmed as active low, the low level will set the interrupt.

3.4 Clocks and Oscillators

The internal 48-MHz oscillator, or the CKIO for synchronous CPU bus operation, can source-clock all the MQ-1100/1132 blocks (see *Figure 3-3*). Additionally, the graphics controller, graphics engine, MIU, CPU interface, USB host, USB function, SPI, and I^2S codec interfaces all contain clock dividers that can be separately programmed for optimal system configuration.

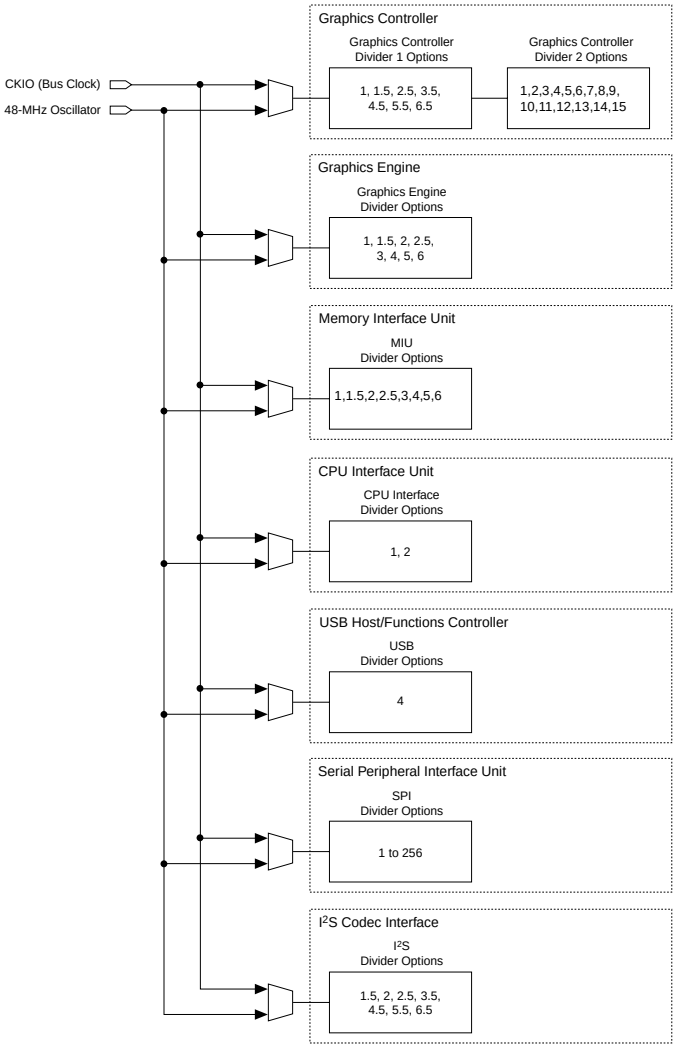


Figure 3-3 Clock and Oscillator Scheme

3.5 Universal Serial Bus (USB)

The USB host port in the MQ-1132 device provides support for both low-speed (1.5 Mbps) and high-speed (12 Mbps) devices. The USB function port (both the MQ-1100 and MQ-1132) is designed to operate at full speed (12 Mbps only). *Figure 3-4,* "MQ-1100/1132 USB Functionality," on page 45, illustrates how one MQ-1100 device port can interface to a USB host port or a USB hub, and how the MQ-1132 USB Host can interface to USB Hub/devices. The power control IC is external circuitry. Typically it's used for gating power from the power supply and/or sensing current direction/draw when the host port is implemented at system level.

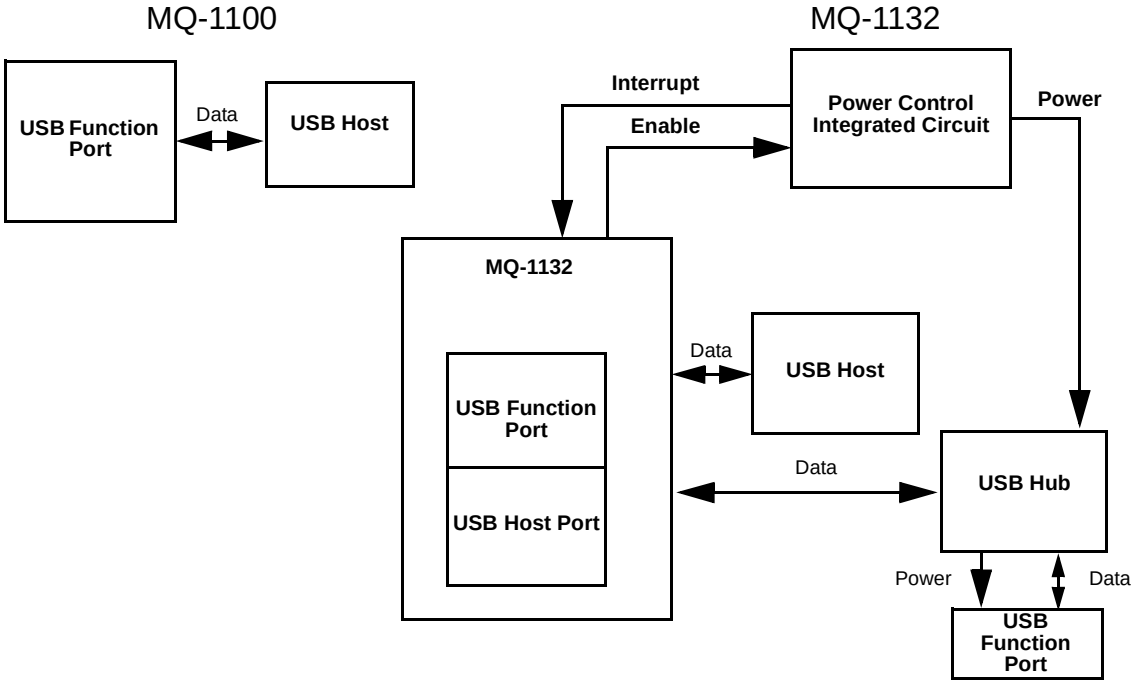


Figure 3-4 MQ-1100/1132 USB Functionality

Communication and data flow on the USB are implemented using endpoints. These uniquely identifiable endpoints are the terminals of communication flow between a USB host and the USB function. Each endpoint has a unique endpoint identifier and a set of registers. You can individually activate each endpoint. The MQ-1100/1132 USB device implements 4 endpoints.

EP0 is the default and control endpoint. EP0 is bi-directional and has two FIFO blocks, one to transmit (IN transactions) and one to receive (OUT transactions). The receiver FIFO block is 4 × 32-bit. This endpoint can receive a transaction of up to 16 bytes. The transmitter FIFO block is 4 × 32-bit and can transmit up to 16 bytes.

EP1 is the interrupt end point and has one 4 × 32-bit FIFO block for transmission. The EP1 endpoint can transmit up to 16 bytes.

EP2 is the BULK/ISO transmitter (IN) end point with a 4 × 64-bit FIFO block that can perform a bulk transfer of up to 64 bytes. Isochronous transfers will be able to transmit more data.

EP3 is the BULK/ISO receiver (OUT Transaction) end point with a 4 × 64-bit FIFO block that can receive a bulk transfer of up to 64 bytes. Isochronous receivers will be able to accept more data.

The EP2 and EP3 endpoints can be configured as BULK or ISO prior to USB enumeration (immediately after USB reset). This is done through UD00R[6:5].

3.6 Serial Peripheral Interface (SPI)

The SPI module (see *Figure 3-5*) is a synchronous serial bus within the MQ-1100/1132. It provides a full-duplex mode of data transfer using three pins, or half-duplex mode of data transfer using two pins. Capable of speeds up to 10 MHz, the SPI can run in either continuous transfer mode or single transfer mode with a programmable time gap between each data transfer. The continuous transfer mode is ideal for devices such as a multi media card (MMC), where an interrupt is only necessary after all the required data has been transferred. The single transfer mode is suitable for devices such as a keyboard or touch-screen controller, where an interrupt is necessary after each data transfer. Enabling or disabling the entire SPI block is possible when not in use in a low-power scenario. If the SPI is not needed, these pins are programmable to operate as GPIO pins.

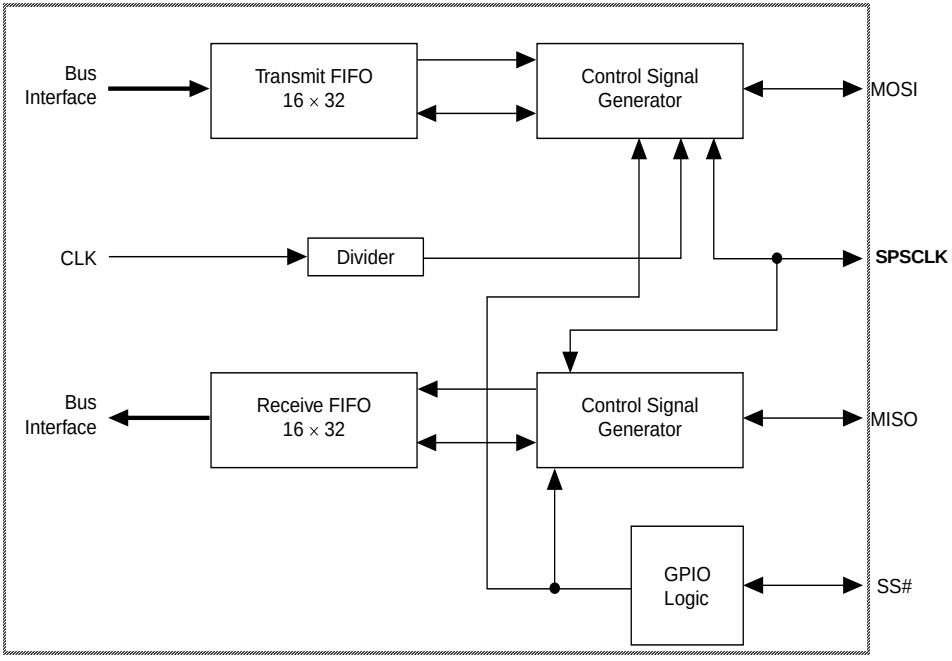


Figure 3-5 MQ-1132 Serial Interface

3.7 I²S Codec Interface

The MQ-1132 offers a codec interface module which supports a super-set of the I²S bus, a serial link developed especially for digital audio systems such as compact disc, digital-audio tape, digital sound processors, and digital TV sound. The I²S bus only handles audio data, while other signals, such as sub-coding and control, are transferred separately (see *Figure 3-6*). Integrated within the MQ-1132 device, the I²S format can send and receive sound data simultaneously as well as act in either a master or slave mode depending on the register configuration. To generate the bit clock, the MQ-1132 contains a clock divider that can divide from one of three sources: the CKIO bus clock, the 48-MHz oscillator, or an externally provided root clock. The codec interface also incorporates direct memory access (DMA) capability to transmit data from on-chip memory to the external codec.

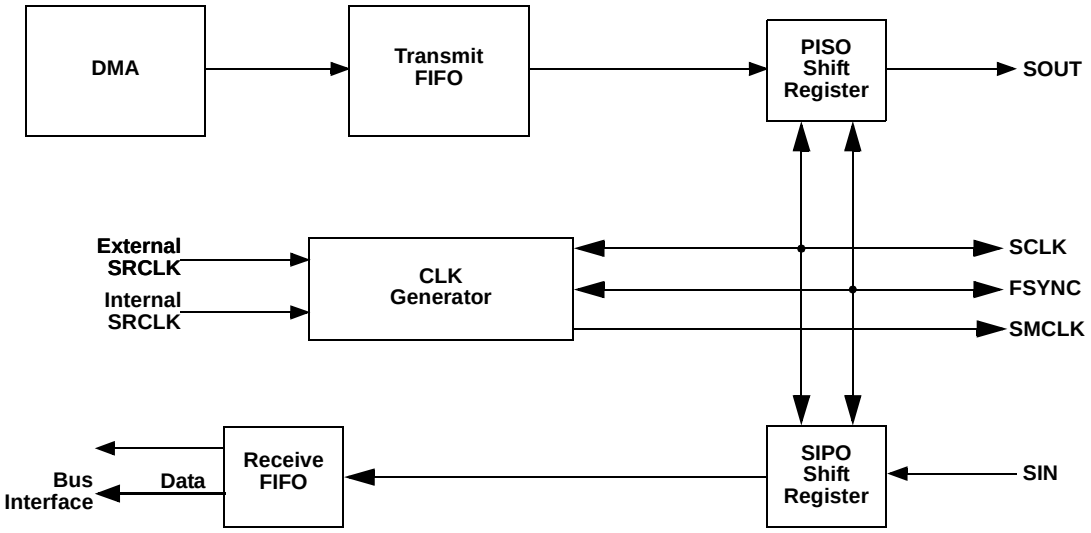


Figure 3-6 I²S Codec Interface

Synchronous serial channel (I^2S) supports three types of interfaces which correspond to the three combinations of the SCLK and FSYNC directions. Table 3-1 lists the interface pins to the external device in the three different modes.

TABLE 3-1: I^2S Interface Pins

Pin	Pin Description	Mode 0 (Slave)	Mode 1	Mode 2 (Master)
SRCLK	Serial root clock input	In	In	In
SMCLK	Serial master clock output	Out	Out	Out
SCLK	Serial bit clock	In	Out	Out
FSYNC	Frame synchronization	In	In	Out
SIN	Serial data in	In	In	In
SOUT	Serial data out	Out	Out	Out

In mode 0 (slave mode), I^2S receives SCLK and FSYNC from external device. In Mode 1, I^2S generates SCLK and receives FSYNC. In mode 2 (master mode), I^2S generates SCLK and FSYNC.

3.8 Graphics Engine

Figure 3-7 illustrates a the MQ-1100/1132 graphics engine block diagram.

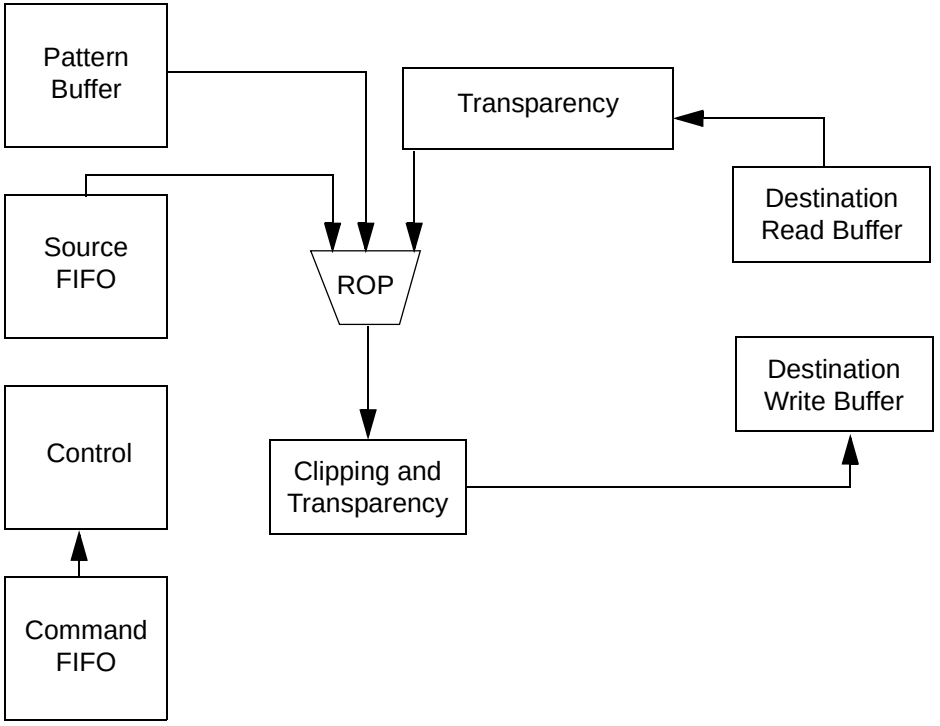


Figure 3-7 Graphics Engine

3.8.1. Theory of Operation

The graphics engine is a specialized logic processor for 2D graphics operations such as BitBLTs and ROPs, area fills, and line drawing. It also provides hardware support for clipping, transparency, rotation, and font color expansion.

The CPU is freed from most of the display rendering function with three main benefits:

- Accelerated graphics operations continue while the CPU is busy, producing smooth screen updates without visible start-and-stop or slow-down motion.
- The graphics engine consumes less power because it is on the same chip as the display buffer. Graphics operations involve the transfer of large amounts of data, and on-chip data transfers consume significantly less power than off-chip transfers. Therefore, graphics engine operations use less power than the CPU would to do the same task.
- The CPU is free to perform time-critical or real-time operations, such as software modem or other I/O functions while the graphics engine renders the graphics.

3.8.2. Raster Operation

In a raster graphics system, objects (such as lines or characters) are first “drawn” in a display memory organized as a Cartesian matrix of pixels, with a direct correspondence between a pixel’s position in the display memory and it’s position on the display. Each horizontal row of pixels is called a raster line. A ROP is a graphics operation that is performed on a rectangular array of pixels. The graphics engine is a 3-operand (source, pattern, destination) raster engine capable of supporting all 256 ROPs as defined for Microsoft operating systems.

Some basic raster operations are:

- BitBLT: a rectangular area of pixels is moved from one location to another.
- Area Fill: a rectangular area is filled with a background color.
- Pattern Fill: an area is filled with a pattern stored in the 8 x 8-pixel pattern buffer.
- Memory-to-Screen Transfer: a BitBLT from a source image to the display memory.

Source data for the raster operation can come from the on-chip display memory or from the main system memory. Source data transfers from system memory are handled either by DMA or by a device driver running on the CPU. Source data can be either monochrome or color. Monochrome source data is expanded to a foreground color or a background color.

Pattern data for the raster operation is an 8 x 8 pixel pattern programmed in the pattern buffer. The MQ-1100 / 1132 only supports monochrome patterns. Monochrome pattern pixels are expanded to a foreground color or a background color. Destination data also can be used as one of the operands for a raster operation, which always comes from the display memory.

3.8.3. Clipping and Transparency

The process of drawing lines, windows, characters, and other objects in the display memory is called rendering. A high-level description of the object (such as the endpoints of a line, for example, or the height, width and origin of a window) is converted into pixels. Rendering is a complex task; it can sometimes be simplified if there is hardware support for clipping and transparency.

The graphics engine provides the following support:

- Clipping: a bounding box is defined, and only pixels inside this box are affected by the graphics operation. Any display modifications outside the bounding box are not written to the display memory, they are clipped.
- Destination Color Transparency: a pixel value is designated as transparent; any pixel output from the graphics engine with this value is not written to the display memory.
- Monochrome Pattern Transparency: either background color or foreground color in the monochrome pattern data can be defined as transparent. A destination pixel corresponding to the specified transparent pattern pixel is not written to the display memory.

Both destination color transparency and monochrome pattern transparency can be simultaneously enabled in a single command. The two transparency controls will be OR’d together.

3.8.4. Bresenham Line Draw

The MQ-1100/1132 can implement the full Bresenham line-drawing algorithm, including arbitrary line draw functionality. It is capable of drawing any non-patterned line of a single-pixel width between any two points on the screen. The MQ-1100/1132 line-draw implementation also supports ROP functions; when a line-draw command is issued, it can be combined with a destination ROP.

3.8.5. Monochrome to Color Expansion

The graphics engine supports pixel resolutions of 8-bpp and 16-bpp. If the source image or pattern image is monochrome (1 bpp), it must be first expanded to match the required pixel resolution. The graphics engine automatically expands a monochrome source or pattern image according to the contents of the foreground and background color registers. When the monochrome source image is font data, this function is sometimes referred to as font expansion. Both source and pattern data can be monochrome data, but the same foreground and background colors will be used.

3.8.6. Graphics Engine Register Set

See *Chapter 4*, for a comprehensive description of these registers.

3.9 Memory Interface Unit

The Memory Interface Unit (MIU) arbitrates requests for memory access from the CPU interface, the graphics engine, the graphics controller, the USB host port, the USB function port, the serial interface, and the I^2S codec interface (see *Figure 3-8*). It also implements the memory sequencer to generate control signals for read/write functionality into the on-chip memory.

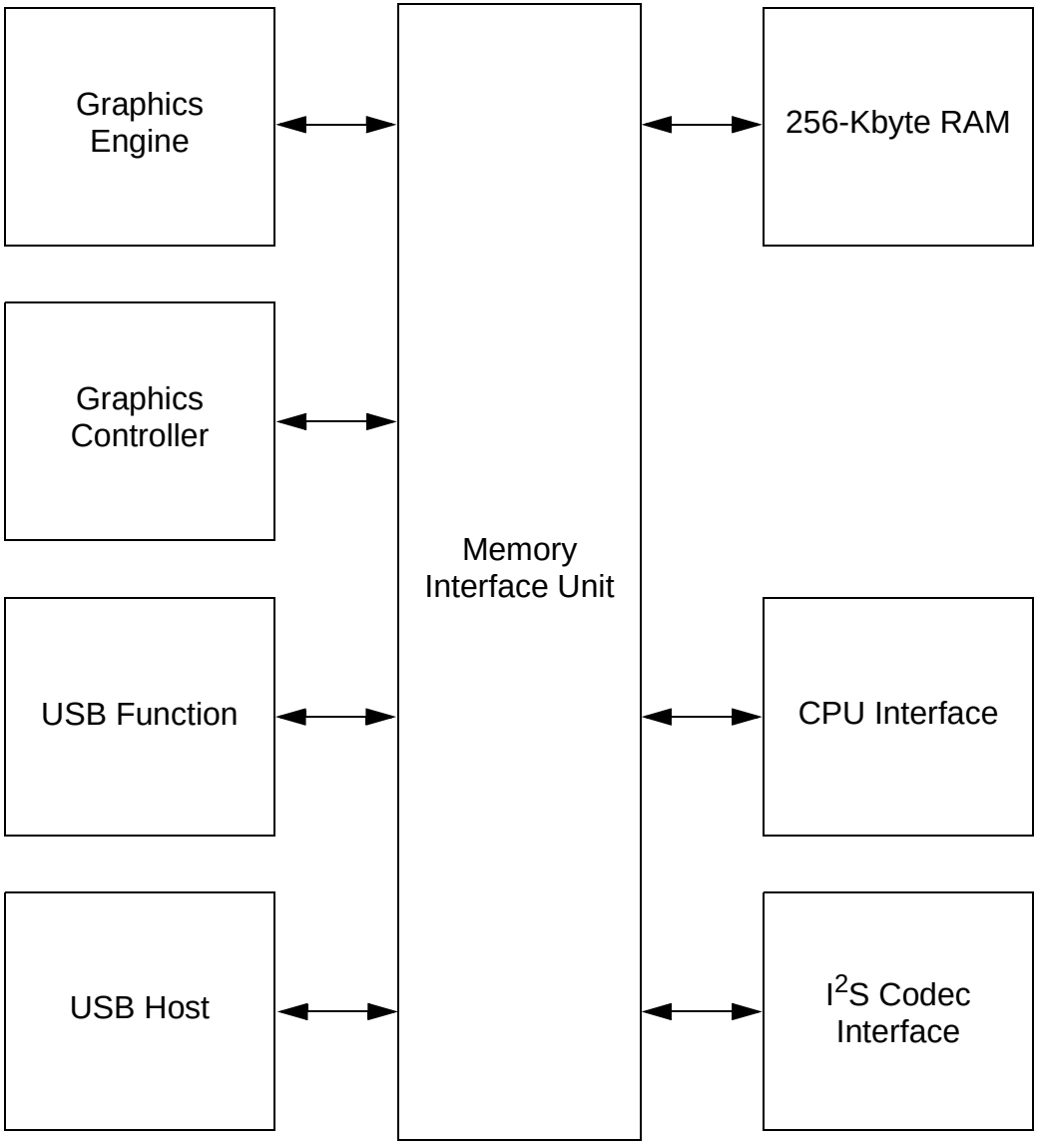


Figure 3-8 Memory Sub-System

3.10 Display Section

The MQ-1100/1132 Graphics Controller and the Flat Panel Interface (FPI) work together to display images. *Figure 3-9* illustrates how these modules are connected. The graphics controller contains a timing generator, a hardware cursor, and a display data FIFO block. The CPU interface module can also read or write to an 18-bit color look-up table (LUT).

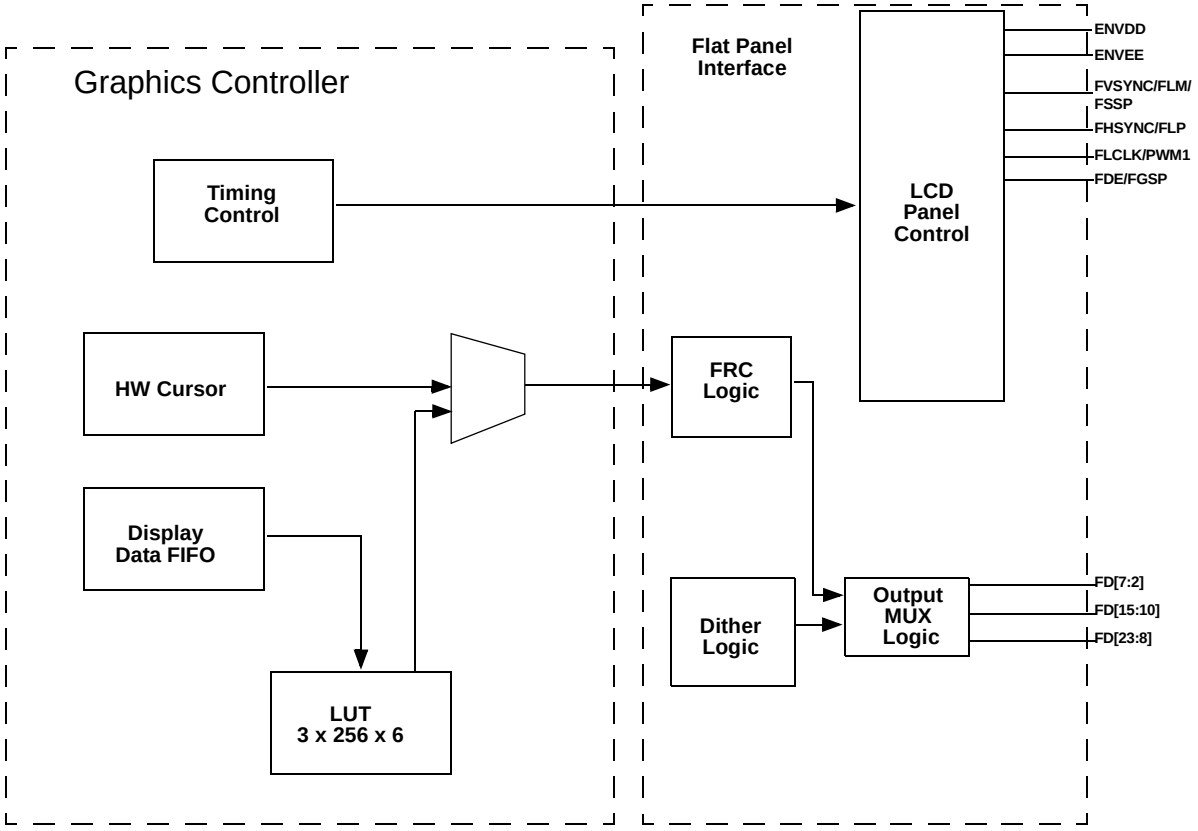


Figure 3-9 Display Path Diagram

3.10.1. Theory of Operation

The graphics controller receives the image data from the on-chip memory and passes it along with timing information to the FPI for display. The graphics controller in the MQ -1100/1132 device generates all the pixel data and the basic timing signals based on resolution and refresh rate required to produce a stable image on the display-output device. The timing signals provide the control signals used by the display device to align the input pixel data with the proper XY position on the display. A set of registers determine the total and active horizontal and vertical sizes of the display with the start-and-end positions of the horizontal and vertical synchronizing signals. These timing signals are then used by the FPI to generate the specific timing signals required for each type of display.

The frame buffer on the MQ-1100/1132 device stores images as an array of pixels. Each pixel specifies the color for one dot in the display. The MQ-1100/1132, LCD and Peripheral Controller supports pixel depths of 1, 2, 4, 8, and 16 bpp. These pixel depths correspond to 2, 4, 16, 256, and 65,536 color choices for each pixel, respectively. For 1, 2, 4, and 8 bpp, each pixel value corresponds to an 18-bit value stored in the color LUT. Pixel data is extracted from the display data FIFO and subsequently used as an index into the LUT to select the 18-bit color value displayed. The LUT must be bypassed for 16 bpp.

3.10.2. Flat Panel Interface

The Flat Panel Interface (FPI) takes 18-bits of digital RGB data and decides what is output from the graphics controller and converts it into data that is provided directly to the flat panel display. The MQ-1100/1132 FPI module supports direct interface to monochrome or color STN panels and monochrome or color TFT panels. A proprietary dithering algorithm is implemented to improve display quality on TFT panels and on STN panels. Also, programmable proprietary grayscaling, FRC, and dithering algorithms are implemented to provide a high-quality display on STN panels. Extensive programmability is built-in to allow fine-tuning of gray scale quality for STN panels.

The internal FRC generates 16 levels of grayscale without dither and 64 levels of grayscale with dither. The pixel clock for the FPI (FPCLK) comes from the graphics controller clock. Flat panel power sequencing is provided as a part of the graphics controller.

The following types of panels are supported:

- 4-, 8-, and 16-bit monochrome S-STN panel
- 4-, 8-, and 16-bit color S-STN panel
- 4-, 6-, and 8-bit monochrome TFT panel
- 9-, 12-, and 18-bit color TFT panel

The FPI only supports 1-pixel per clock panels for TFT panels. The maximum FPI pixel clock frequency is 48 MHz for both TFT and STN panels. The pins used for the FPI serve different functions according to the programmed panel type.

3.10.3. Signal to Pin Mapping for Color and Monochrome Panels

Table 3-2 and *Table* 3-3, "Signal Pin Mapping for Monochrome Panels," on page 56, summarize the pin and signal-mapping for the supported panel types.

TABLE 3-2: Signal Pin Mapping for Color Panels

Pin Name	TFT 18 Bits	TFT 12 Bits	TFT 9 Bits	S-STN 16 Bits	S-STN 8 Bits	S-STN 4 Bits
FD23	R5	R3	R2	UR0	UR0	UR0
FD22	R4	R2	R1	UR1	UR1	UR1
FD21	R3	R1	R0	UR2	UR2	
FD20	R2	R0		UR3		
FD19	R1			UR4		
FD18	R0			UR5		
FD15	G5	G3	G2	UG0	UG0	UG0
FD14	G4	G2	G1	UG1	UG1	
FD13	G3	G1	G0	UG2	UG2	
FD12	G2	G0		UG3		
FD11	G1			UG4		
FD10	G0					
FD7	B5	B3	B2	UB0	UB0	UB0
FD6	B4	B2	B1	UB1	UB1	
FD5	B3	B1	B0	UB2		
FD4	B2	B0		UB3		
FD3	B1			UB4		
FD2	B0					
FVSYNC	FVSYNC	FVSYNC	FVSYNC	FLM	FLM	FLM
FHSYNC	FHSYNC	FHSYNC	FHSYNC	LP	LP	LP
FDE	FDE	FDE	FDE	—	—	—
FMOD	FMOD	FMOD	FMOD	FMOD	FMOD	FMOD
FSCLK	FSCLK = FPCLK	FSCLK = FPCLK	FSCLK = FPCLK	FSCLK = (FPCLK **x** 3)/16	FSCLK = (FPCLK **x** 3)/8	FSCLK = (FPCLK **x** 3)/4

TABLE 3-3: Signal Pin Mapping for Monochrome Panels

Pin Name	TFT 8 Bits	TFT 6 Bits	TFT 4 Bits	S-STN 16 Bits	S-STN 8 Bits	S-STN 4 Bits
FD23				UD6	UD6	
FD22				UD7	UD7	
FD21						
FD20				UD14		
FD19				UD15		
FD18						
FD15	P1			UD0	UD0	UD0
FD14	P0			UD1	UD1	UD1
FD13				UD2	UD2	UD2
FD12				UD3	UD3	UD3
FD11				UD4	UD4	
FD10				UD5	UD5	
FD7	P7	P5	P3	UD8		
FD6	P6	P4	P2	UD9		
FD5	P5	P3	P1	UD10		
FD4	P4	P2	P0	UD11		
FD3	P3	P1		UD12		
FD2	P2	P0		UD13		
FVSYNC	FVSYNC	FVSYNC	FVSYNC	FLM	FLM	FLM
FHSYNC	FHSYNC	FHSYNC	FHSYNC	LP	LP	LP
FDE	FDE	FDE	FDE	—	—	—
FMOD	FMOD	FMOD	FMOD	FMOD	FMOD	FMOD
FSCLK	FSCLK = FPCLK	FSCLK = FPCLK	FSCLK = FPCLK	FSCLK = FPCLK/16	FSCLK = FPCLK/8	FSCLK = FPCLK/4

3.10.4. Timing Diagrams for STN Panels

Figure 3-10 through *Figure 3-15,* "16-Bit Monochrome S-STN," on page 61, illustrate the timing diagrams for the panels supported by the MQ-1100/1132, LCD and Peripheral Controller.

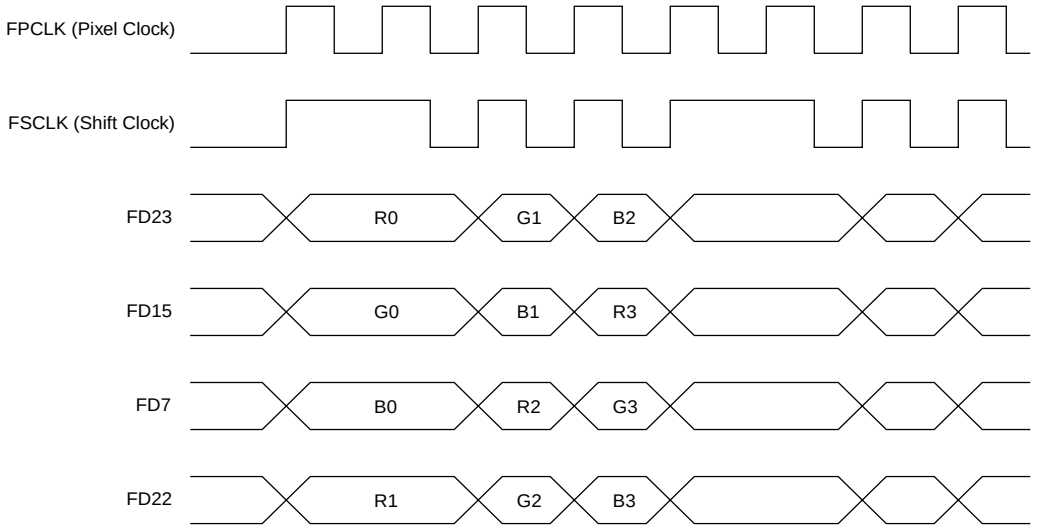


Figure 3-10 4-Bit Color S-STN

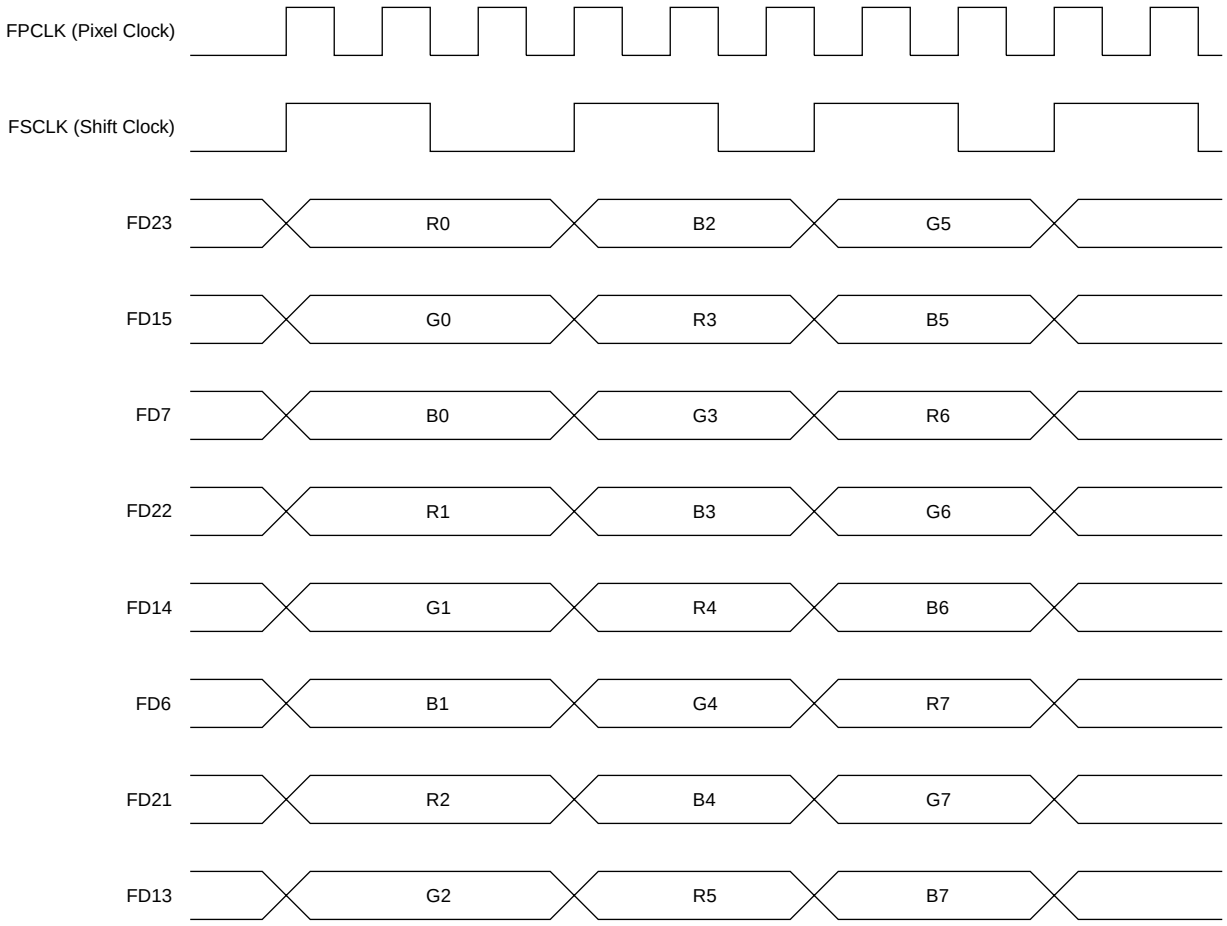


Figure 3-11 8-Bit Color S-STN

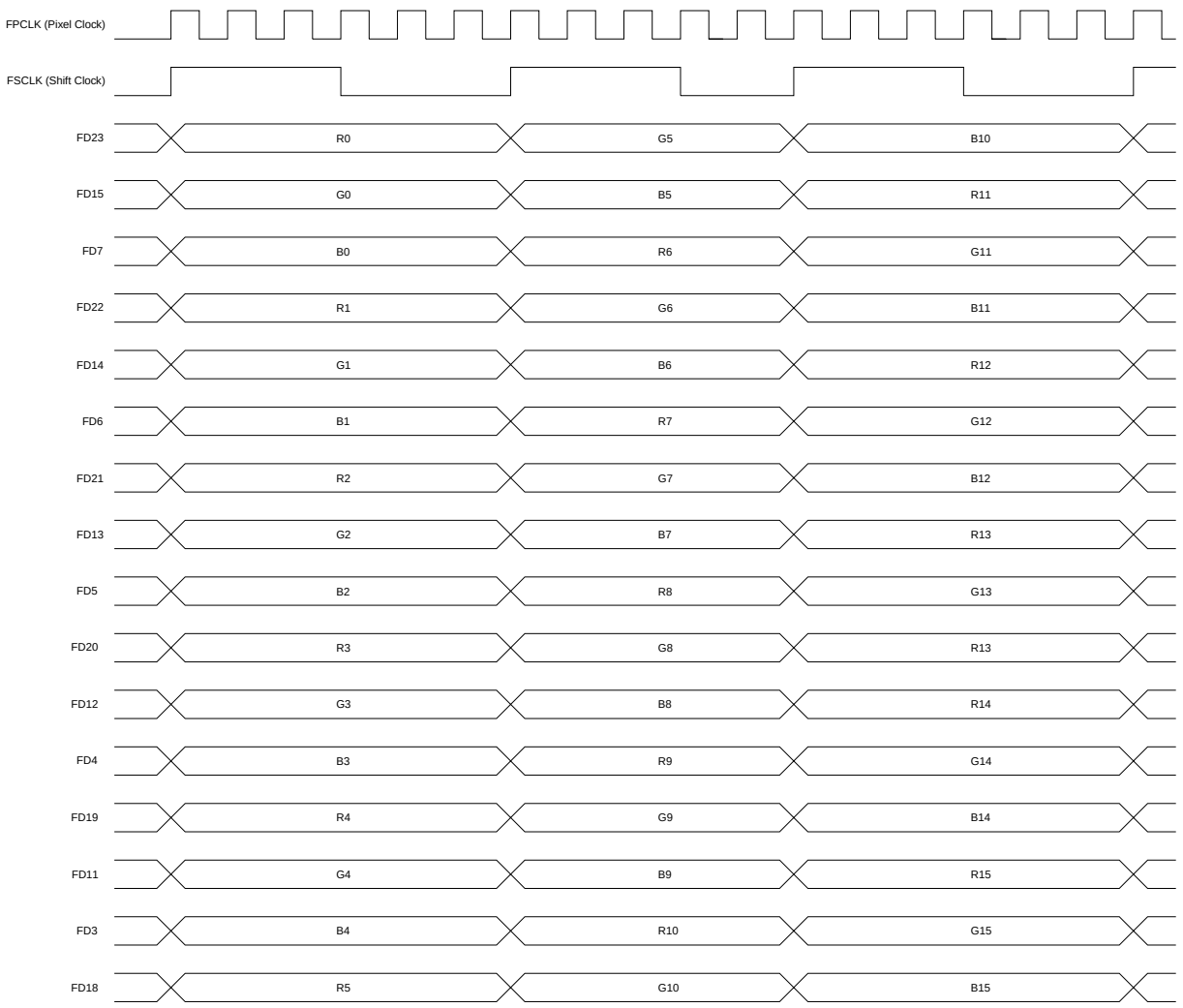


Figure 3-12 16-Bit Color S-STN

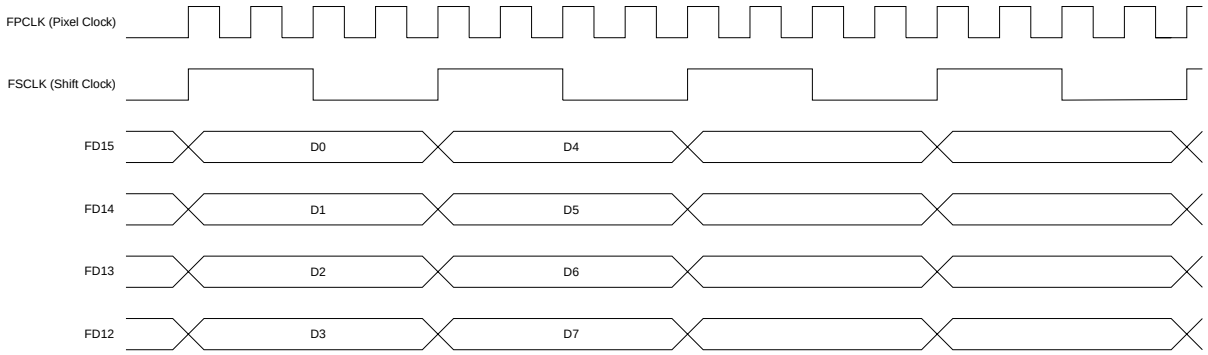


Figure 3-13 4-Bit Monochrome S-STN

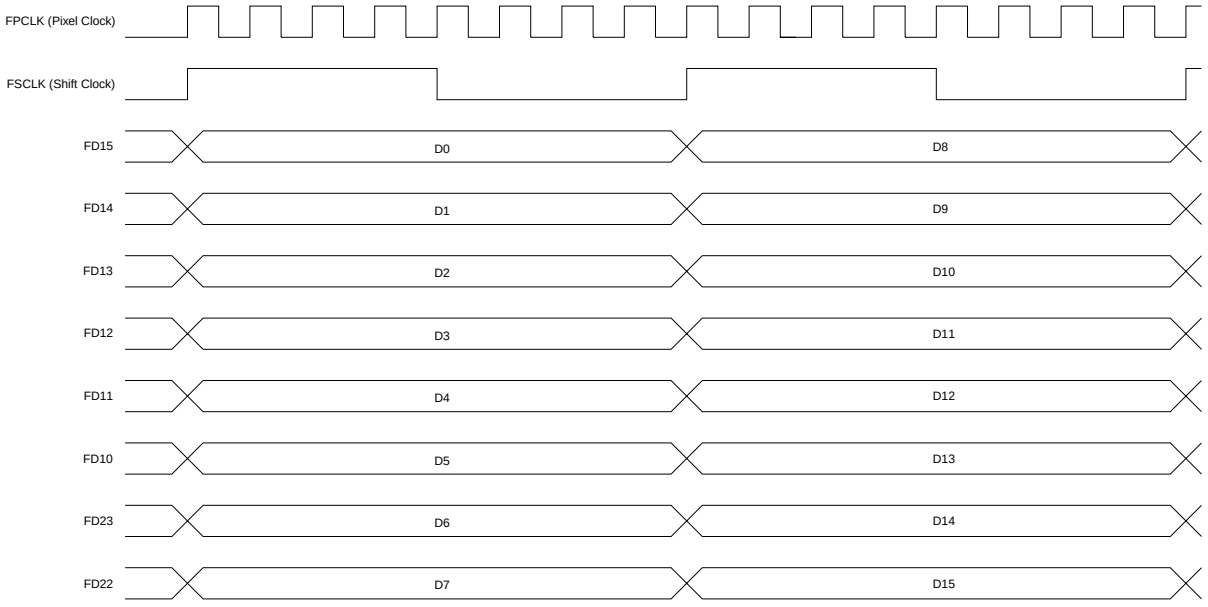


Figure 3-14 8-Bit Monochrome S-STN

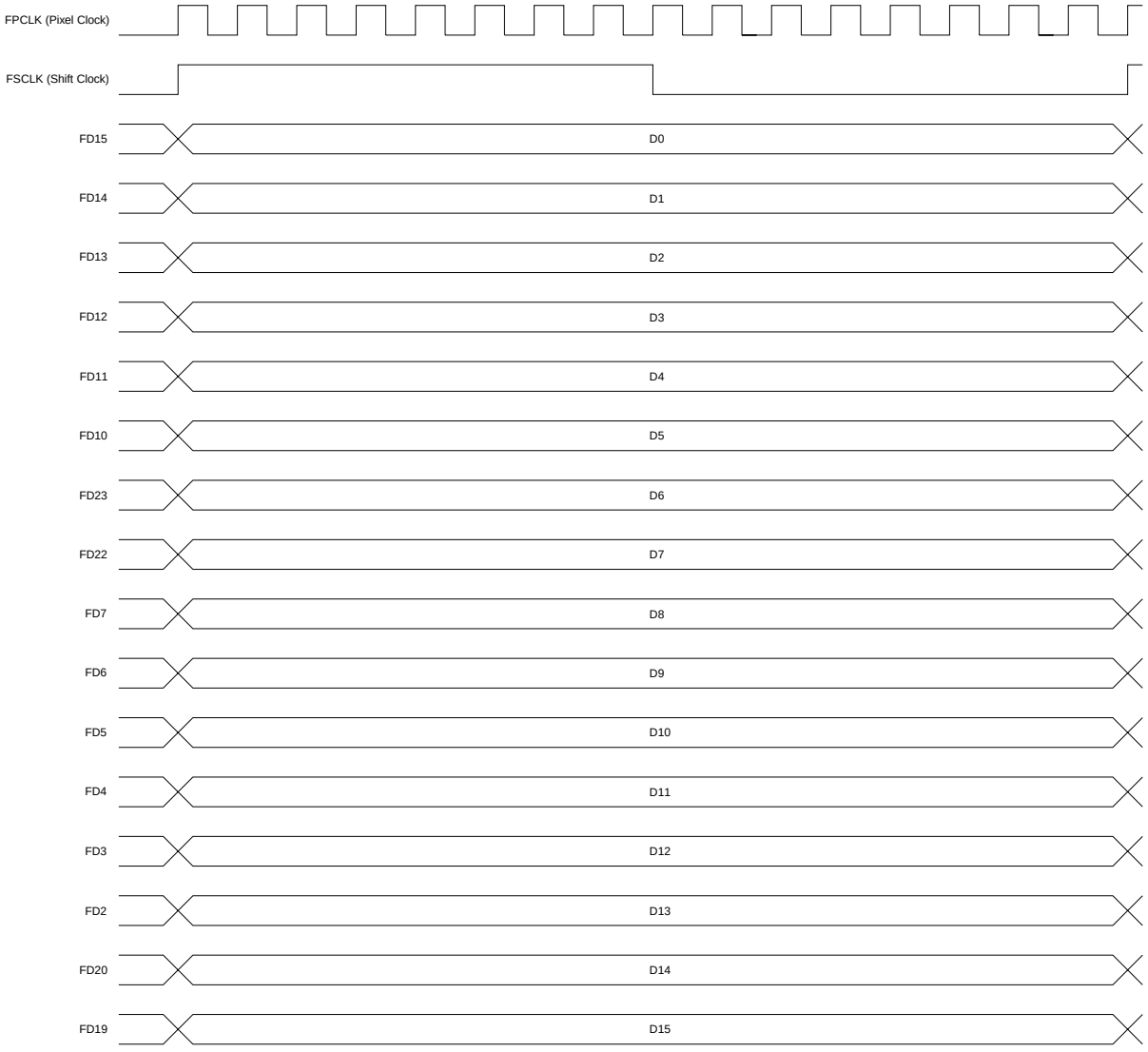


Figure 3-15 16-Bit Monochrome S-STN

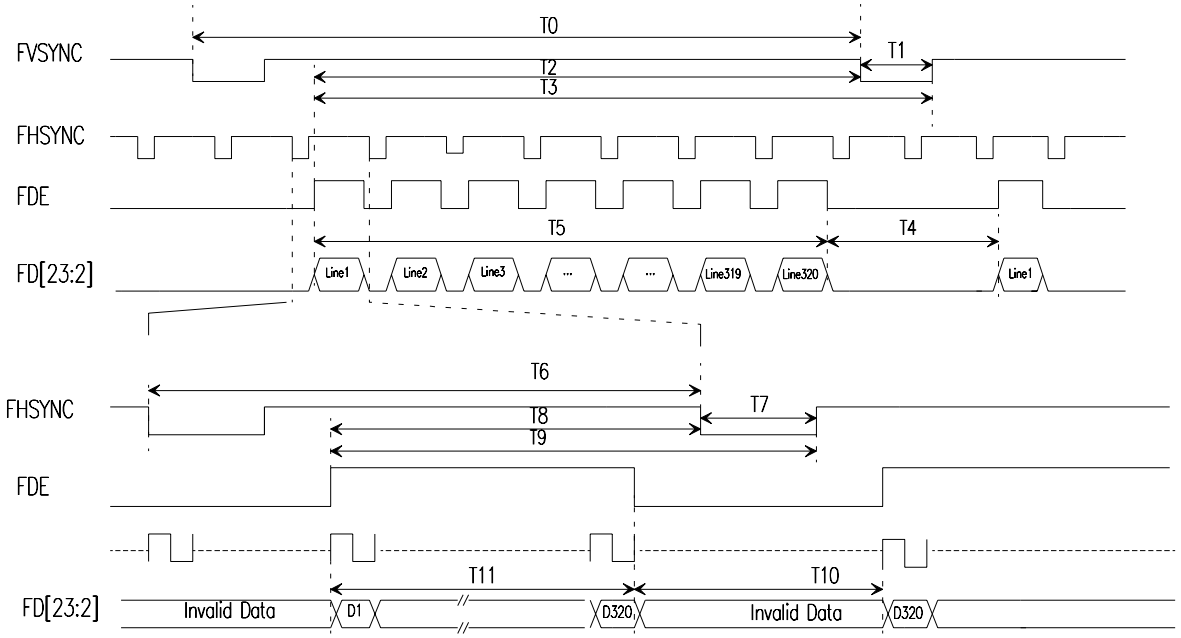


Figure 3-16 Generic TFT Timing

TABLE 3-4: 320 x 320 TFT Panel Horizontal and Vertical Timings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Vertical Total	T0	VT			Lines
Vertical Sync Width	T11	1			Lines
Vertical Sync Start	T2	VSS			Line
Vertical Sync End	T3	VSE			Lines
Vertical Blank Time	T4	VBT			Lines
Vertical Display End	T5	VDE			Lines
Horizontal Total	T6	HT			Pixel Clock
Horizontal Sync Width	T7	1			Pixel Clock
Horizontal Sync Start	T8	HSS			Pixel Clock
Horizontal Sync End	T9	HSE			Pixel Clock
Horizontal Blank Time	T10	HBT			Pixel Clock
Horizontal Display End	T11	HDE			Pixel Clock

Chapter 4

4-1. Programming Information

4.2 MQ-1100/1132 Address Map (Microprocessor Interfaces)

The MQ-1100/1132 connects directly to microprocessors that support a logical address space and a physical address space. The physical address range is decoded internally by the CPU, which generates the chip select(s) and drives the address bus. Microprocessors supported by the MQ-1100/1132 include: the Hitachi SH-7709 and SH-7750, NEC VR-4121, VR-4111 and VR-4122 (by means of and I/O (LCD) interface), Intel SA-1110 and Xscale-based CPU and the Motorola Dragonball series (MC68EZ328, MC68VZ328). The MQ-1100/1132 requires 512 Kbyte of address space. This address space is broken into three regions. The lower 256 Kbyte region maps to the 256 Kbyte internal SRAM and contains the graphics frame buffer. Data in this region is used to refresh the display. The amount used for display purposes depends on the display resolution and color depth. Accesses to this region are serialized so that if the graphics engine is drawing to the frame buffer, CPU reads/writes are held off. The next region is the 8 Kbyte register space, which is located just above the frame buffer. The third region, consisting of the remaining 248 Kbyte of address space is also mapped to the upper 248 Kbyte of internal SRAM. Accesses to this address space are not serialized with graphics engine accesses. This address space is used to access non-graphics frame buffer memory such as buffers for USB, Audio, etc.

Figure 4-1 illustrates the mapping of the microprocessor address space to the embedded SRAM and memory mapped registers in the MQ-1100/1132 for local bus interfaces.

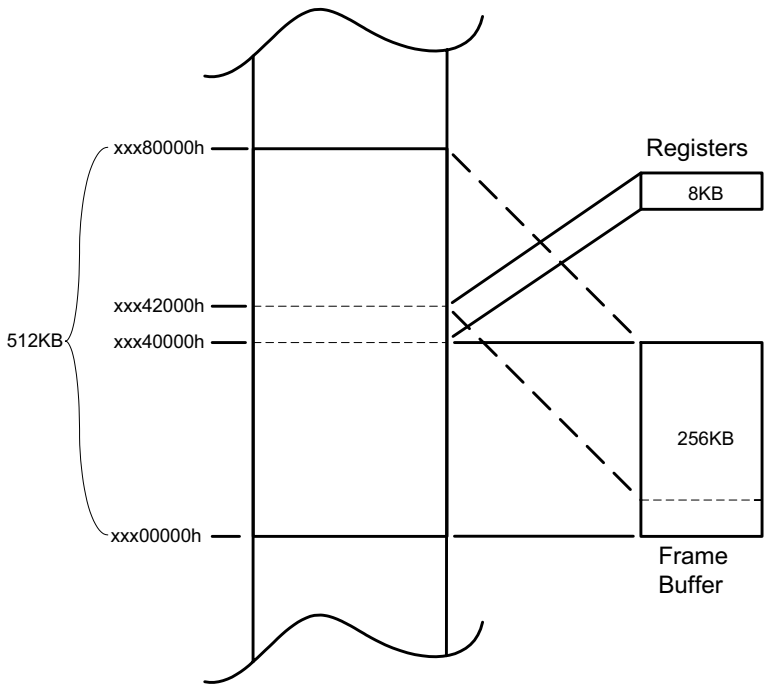


Figure 4-1. CPU Address Mapping

4.3 MQ-1100/1132 Address Map (PCI)

The MQ-1100/1132 also supports a direct connection to PCI. Two separate address spaces are defined using Base Address Register 0 (BAR 0) and Base Address Register 1 (BAR 1). Both BAR 0 and BAR 1 claim 512KB of system address space.

The register space of the MQ-1100/1132 is located in the lower 8KB of BAR 0. The remaining 504K is unused and will return undefined values if read. BAR 1 is also 512KB in size and is split into two 256KB regions. The lower 256KB region maps to the 256KB internal SRAM and contains the graphics frame buffer. Data in this region is used to refresh the display. The amount used for display purposes depends on the display resolution and color depth. Accesses to this region are serialized. This means that if the graphics engine (GE) is drawing to the frame buffer, CPU reads/writes are held off. The upper 256KB region also maps to the 256KB of internal SRAM. Accesses to this address space are not serialized with GE activity. This address space is used to access non-graphics frame buffer memory such as buffers for USB Audio, etc.

Figure 4-2 illustrates the mapping of the PCI Base Addresses to the embedded SRAM and memory mapped registers in the MQ-1100/1132.

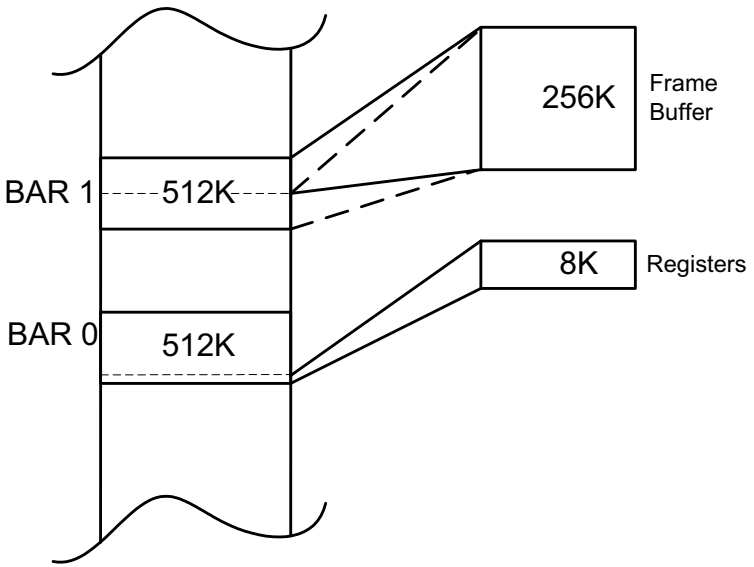


Figure 4-2. PCI Address Mapping

4.4 Register Mapping

TABLE 4-1: MQ-1100/1132 Register Mapping

MQ-1100/1132 Register Mapping	Address Range (19-bit hex address in bytes)
CIF Module – 128 Bytes	0x000 to 0x07F
Memory Controller – 128 Bytes	0x080 to 0x0FF
Interrupt Controller – 128 Bytes	0x100 to 0x17F
Graphics Controller – 128 Bytes	0x180 to 0x1FF
Graphics Engine – 128 Bytes	0x200 to 0x27F
Synchronous Serial Controller – 128 Bytes	0x280 to 0x2FF
Serial Peripheral Interface (SPI) – 128 Bytes	0x300 to 0x37F
Device Configuration Space – 128 Bytes	0x380 to 0x3FF
PCI Configuration Header – 256 Bytes	0x400 to 0x4FF
USB Host – 256 Bytes	0x500 to 0x5FF
Flat Panel Controller – 512 bytes	0x600 to 0x7FF
Color Palette – 1024 bytes	0x800 to 0xBFF
Source FIFO Space – 1024 bytes	0xC00 to 0xFFF
USB Device – 128 Bytes	0x1000 to 0x107F

4.5 Registers Implemented in the CPU Configuration Module

4.5.1. Device Configuration Registers

The following specifies the index, offset and reset values for the device configuration registers.

TABLE 4-2: Device Configuration Register Index and Reset Values

Register	Index	Offset	Reset Value	See Description
DC00R	00h	380h	0000-0000h	*Register 4-1 on page 66*
DC01R	04h	384h	F000-000h	*Register 4-2 on page 67*
DC02R	08h	388h	0000-0000h	*Register 4-3 on page 68*
DC03R	0Ch	38Ch	0000-0000h	*Register 4-4 on page 68*
DC04R	10h	390h	0000-0000h	*Register 4-5 on page 68*
DC05R	14h	394h	0000-0000h	*Register 4-6 on page 70*
DC06R	18h	398h	0000-0000h	*Register 4-7 on page 70*
DC07R	1Ch	39Ch	0000-0000h	*Register 4-8 on page 70*

Device configuration register 0 (DC00R) should be written before any other register or memory accesses if the default value of this register requires modification. The default value of this register changes depending on the processor interface in use. DC00R has no meaning for PCI interface. The default values for this register are:

00–Big endian mode is enabled with 16-bit byte swapping for DragonBall-EZ interface

X1–Little endian mode with no byte swapping for all the other supported processor bus interfaces

Software should always write 16-bit data into DC00R to modify the default value. Replicate the two data value bits written into DC00R in 16-bit input. For example, software should write 1010101010101010 into this register to update DC00R[1:0] with a value of 10. *Register 4-1* specifies the DC00R bit values and definitions.

Register 4-1: Device Configuration Register 0 (DC00R: Index 00h, Offset 380h)

Bit	Bit Definition	Bit Value	Value Definition
0	Little endian mode enable.	0	Enable big endian mode. Byte swapping is performed on input and output data because the MQ-1100/1132 always operates in little endian format. The type of byte swapping performed is specified by DCC00R[1].
		1	Enable little endian mode. Byte swapping is not performed on data.
1	Byte swapping mode. This bit is only effective if DC00R[0] = 0.	0	Enable 16-bit Byte swapping for big endian to little endian conversion. byte0 <-> byte1, byte2 <-> byte3
		1	Enable 32-bit byte swapping for big endian to little endian conversion. byte0 <-> byte3, byte1 <-> byte2
31:2	Reserved bits		

Device configuration register 1 (DC01R) is accessible all the time (even if all the internal clocks are disabled) for all the bus interfaces supported by the MQ-1100/1132. *Register 4-2* specifies the DC01R bit values and definitions.

Register 4-2: Device Configuration Register 1 (DC01R: Index 04h, Offset 384h)

Bit	Bit Definition	Bit Value	Value Definition
1:0	1.8 Volt Oscillator	00	1.8 volt oscillator is disabled. Complete power down mode.
		01	1.8 volt oscillator bypass mode. Internal oscillator is bypassed and powered down. External oscillator driving OSCFO should be used.
		10	Reserved
		11	1.8 volt internal oscillator with external crystal enabled.
4:2	Reserved.		Must be programmed to 0.
7:5	Reserved		
8	CPU interface clock divisor. This parameter determines the 48-MHz oscillator output clock divisor factor to generate the CPU and bus interface clock for systems where this clock is not provided externally.	0	CPU interface clock is the oscillator clock divided by 1.
		1	CPU interface clock is oscillator clock divided by 2.
9	DTACK control for DragonBall bus interface. This parameter controls the DTACK generation for read cycles only.	0	DTACK is driven in the same clock cycle as bus-interface read data is latched out.
		1	DTACK is driven one cycle after bus-interface read data is latched out.
10	StrongARM interface synchronizer control. This parameter determines how fast the StrongARM bus interface signals are synchronized internally.	0	Must be programmed to 0 if the CPU clock is less than 32 MHz
		1	Must be programmed to 0 if the CPU clock is greater than 32 MHz
	NEC interface: Delay sampling of next cycle in case of fast back to back or burst cycle	0	Must be programmed to 0 if the CPU clock is greater than the CPU interface clock
		1	Must be programmed to 0 if the CPU clock is less than the CPU interface clock
11	Write data latch control for DragonBall bus interface. This parameter controls bus data latching.	0	Use this setting if the internal-bus clock is 48 MHz or the processor speed is slower than 24 MHz.
		1	Use this setting if the internal-bus clock is 24 MHz and the processor speed is 24 MHz or faster.
12	CPU interface test mode enable This bit should be set only during test mode	0	CPU test mode is disabled
		1	CPU test mode enabled.
15:13	Reserved		
16	Software chip reset. Setting this bit resets the chip except for the bus-interface unit.	0	Software reset is disabled.
		1	Software reset is enabled.
27:17	Reserved		
28	Weak pull-down control for flat-panel pin FMOD.	0	Disable weak pull-down.
		1	Enable weak pull-down.
29	Weak pull-down control for flat-panel pin FLCLK.	0	Disable weak pull-down.
		1	Enable weak pull-down.
30	Weak pull-down control for flat-panel pin PWM0.	0	Disable weak pull-down.
		1	Enable weak pull-down.
31	Weak pull-down control for flat-panel pin PWM1.	0	Disable weak pull-down.
		1	Enable weak pull-down.

Device configuration register 2, DC02R, is continuously accessible. *Register 4-3* specifies the DC02R bit values and definitions.

Register 4-3: Device Configuration Register 2 (DC02R: Index 08h, Offset 388h)

Bit	Bit Definition	Bit Value	Value Definition
0	CPU configuration (CC) module enable.	0	Disable CC module. The MQ-1100/1132 only responds to register accesses for the PCI vendor-ID register. DC00R, DC01R, DC02R, and DC03R. CC block internal clocks are disabled. Bus state machine clocks are active for synchronous bus interfaces, but they respond to the registers mentioned above.
		1	CC module: All the bus accesses in the MQ-1132 enable address range are responded. All the clocks generated in the CC block are enabled.
31:1	Reserved		

Device configuration register 3 (DC03R) is readable all the time. *Register 4-4* specifies the DC03R bit values and definitions.

Register 4-4: Device Configuration Register 3 (DC03R: Index 0Ch, Offset 38Ch)

Bit	Bit Definition	Bit Value	Value Definition
6:0	Bus-interface mode (read only). This parameter returns the current bus interface mode.	0000001	SH-7750 mode
		0000010	SH-7709 mode
		0000100	VR-4111 and VR 4121 mode.
		0001000	SA-1110 mode.
		0100000	PCI mode (MQ-1132 only)
		1000000	DragonBall-EZ mode.
		All others	Reserved.
31:7	Reserved		

Device configuration register 4 (DC04R) is accessible only if DC02R[0] is 1. *Register 4-5* specifies the DC04R bit values and definitions.

Register 4-5: Device Configuration Register 4 (DC04R: Index 10h, Offset 390h)

Bit	Bit Definition	Bit Value	Value Definition
0	Graphics engine force busy (global). This bit is effective when DC05R[0] is set. Setting this bit disables the graphics engine's global dynamic power management so the engine is not automatically shut off when it is idle.	0	Graphics engine clock is powered down when there is no activity.
		1	Graphics engine clock is always running.
1	Graphics engine force busy (local). This bit is effective when DC05R[0] is set. Setting this bit to disable the local dynamic power management for the graphics engine pipelines so the individual pipeline is not automatically shut off when it is idle.	0	Graphics engine pipeline is powered down when there is no activity.
		1	Graphics engine pipeline is always running.
2	Graphics engine clock select. These bits select the graphics engine clock.	0	Graphics engine is driven by the bus-interface clock.
		1	Graphics engine is driven by the 48-MHz oscillator clock.

Register 4-5: Device Configuration Register 4 (DC04R: Index 10h, Offset 390h)

Bit	Bit Definition	Bit Value	Value Definition
5:3	Graphics engine clock divider. This parameter controls the clock divider for the graphics engine.	000	Divide the clock by 1.
		001	Divide the clock by 1.5.
		010	Divide the clock by 2.
		011	Divide the clock by 2.5.
		100	Divide the clock by 3.
		101	Divide the clock by 4.
		110	Divide the clock by 5
		111	Divide the clock by 6.
6	Graphics engine command FIFO reset. This bit is effective independent of bit 8.	0	Enable graphics engine command FIFO.
		1	Resets graphics engine command FIFO.
7	Graphics engine CPU source FIFO reset. This bit is effective independent of bit 8.	0	Enable graphics engine CPU source FIFO.
		1	Resets graphics engine CPU source FIFO.
8	USB host controller SE0 bus state detection enable during global suspend mode. This bit is used in USB host clock gating if the global suspend mode is active. (MQ-1132 only)	0	Disable SE0 detection during global suspend mode to initiate remote wakeup.
		1	Enable SE0 detection during global suspend mode to initiate remote wakeup.
9	USB host controller dynamic power feature enable. (MQ-1132 only)	0	Disable automatic clock disabling for 48-MHz clock.
		1	Enable automatic clock disabling for 48-MHz clock. When this bit is 1, the USB device controller clock is Disabled as soon as it detects global suspend.
10	USB counter-scale enable. Set this bit to 0 during normal operation. (factory test mode)	0	Use real-time value to generate 1-ms time period.
		1	1-ms duration (12,000 clocks of Clk12) is scaled down to 7 clocks of Clk12. This is used for simulation purposes.
11	USB-host read test-mode enable. Set this bit to 0 during normal operation. (factory test mode)	0	Disable test mode.
		1	Enable test mode.
15:12	USB host controller test-mode data source select. (factory test mode)		
16	USB transceiver test-mode enable. Set this bit to 0 during normal operation. (factory test mode)	0	Disable test mode.
		1	Enable test mode.
17	USB over-current detection enable for USB host controller. When this bit is set to 1, USB over-current detection is enabled through GPIO pin 25.	0	Disable over-current detection.
		1	Enable over-current detection.
18	USB device controller dynamic power feature enable.	0	Disable automatic clock disabling for 48-MHz clock.
		1	Enable automatic clock disabling for 48-MHz clock. When this bit is 1, the USB host controller clock is disabled when it detects global suspend.
19	USB host transceiver input enable. (MQ-1132 only)	0	Disable all transceiver inputs.
		1	Enable all transceiver inputs.
20	USB device transceiver input enable. (factory test mode)	0	Disable all transceiver inputs.
		1	Enable all transceiver inputs.
21	USB host and device test vector generation mode enable. (factory test mode)	0	Disable USB test vector generation mode.
		1	Enable USB test vector generation mode.
31:22	Reserved		

Device configuration register 5 (DC05R) is accessible only if DC02R[0] is 1. *Register 4-6* specifies the DC05R bit values and definitions.

Register 4-6: Device Configuration Register 5 (DC05R: Index 14h, Offset 394h)

Bit	Bit Definition	Bit Value	Value Definition
0	Graphics engine enable. This bit controls the graphics engine. Program this register after the DC04R register.	0	Graphics engine is powered down. All graphics-engine related logic (state machines, command FIFO, source FIFOs, etc.) is reset.
		1	Graphics engine is enabled. You can normally set this bit at any time because the graphics engine can be automatically powered down when there is no activity.
1	USB host enable. This bit enables the 48-MHz clock used in the USB host controller. (MQ-1132 only)	0	Disable the 48-MHz USB host controller input clock.
		1	Enable the 48-MHz USB host controller input clock.
2	USB device clock enable. This bit enables the USB device clock.	0	Disable USB device controller's 48-MHz input clock.
		1	Enable USB device controller's 48-MHz input clock.
31:3	Reserved		

Software register 6 (DC06R) is accessible only if DC02R[0] is 1. *Register 4-7* specifies the DC06R bit values and definitions.

Register 4-7: Device Configuration Register 6 (DC06R: Index 18h, Offset 398h)

Bit	Bit Definition	Bit Value	Value Definition
31:0	Software register 0. This is only used by the drivers.		

Software register 7, DC07R, is accessible only if DC02R[0] is 1. *Register 4-8* specifies the DC07R bit values and definitions.

Register 4-8: Device Configuration Register 7 (DC07R: Index 1Ch, Offset 39Ch)

Bit	Bit Definition	Bit Value	Value Definition
31:0	Software register 1. This is only used by the drivers.		

4.5.2. CPU Interface Registers

All CPU interface registers are accessible only if DC02R[0] is programmed as 1.

Table 4-3 specifies the index, offset and reset values for the CPU interface registers.

TABLE 4-3: CPU Interface Registers

Register	Index	Offset Value	Reset Value	See Description
CC00R	00h	000h	0000-0000h	*Register 4-9 on page 71*
CC01R	04h	004h	0000-0000h	*Register 4-10 on page 72*
CC02R	08h	008h	0000-0000h	*Register 4-11 on page 73*
CC03R	0Ch	00Ch	0000-0000h	*Register 4-12 on page 76*
CC04R	10h	010h	0000-0000h	*Register 4-13 on page 78*

Register 4-9 through *Register 4-13* describe the CPU interface register bit values and definitions.

Register 4-9: CPU Control Register (CC00R: Index 00h, Offset 000h)

Bit	Bit Definition	Bit Value	Value Definition
0	MIU read request "generator on" for one transaction.	0	CIF generates a read request to the MIU only when there is a cache miss. CIF keeps track of the CPU writes to the Frame Buffer to validate the cached data. CIF guarantees cache coherency if the frame buffer is accessed by the CPU only. If the graphics engine modifies the data in the frame buffer, then CIF does not guarantee the correct data being read The previously cached data may be from the same address where the graphics engine modified and the CPU tries to read that address.
		1	Setting this bit forces a read request by the CIF to the MIU regardless of the validity bits. This bit is automatically cleared once the read request is made. Software writes a 1 to this bit whenever it reads the data from the frame buffer modified by the graphics engine. Software only writes a 1 for the first read. For subsequent reads, after one graphics engine command is executed, software does not need to set this bit.
1	Disable read cache associated with the frame buffer reads.	0	Read request to the MIU is generated only if the requested read data from the frame buffer is not cached.
		1	Read request to the MIU is generated for every read transaction initiated by the host whether the requested read data from the frame buffer is cached or not. This bit must be cleared or only set by the software.
2	Reserved		
3	CLKRUN enable.	0	Disable CLKRUN
		1	Enable CLKRUN
5:4	GPIO source data select for GPIO[25:20] and GPIO[7:0]. These bits are used for testing. (factory test mode)	00	Source data comes from the USB host controller or the USB device.
		01	Source data comes from the memory interface controller.
		10	Source data comes from the CPU interface controller.
		11	Reserved.
7:6	CPU interface GPIO data (factory test mode)		
31:8	Reserved		

Register 4-10: Source FIFO/Command FIFO/Graphics Engine Status Register (CC01R: Index 04h, Offset 004h)

Bit	Bit Definition	Bit Value	Value Definition
4:0	Command FIFO status (CFS) register. Command FIFO is 16-entries deep.	00000	Command FIFO is full.
		00001	Command FIFO has one location free.
		00010	Command FIFO has two locations free.
		00011	Command FIFO has three locations free.
		00100	Command FIFO has four locations free.
		00101	Command FIFO has five locations free.
		00110	Command FIFO has six locations free.
		00111	Command FIFO has seven locations free.
		01000	Command FIFO has eight locations free.
		01001	Command FIFO has nine locations free.
		01010	Command FIFO has ten locations free.
		01011	Command FIFO has eleven locations free.
		01100	Command FIFO has twelve locations free.
		01101	Command FIFO has thirteen locations free.
		01110	Command FIFO has fourteen locations free.
		01111	Command FIFO has fifteen locations free.
		10000	Command FIFO is empty.
7:5	Reserved		
12:8	Source FIFO status (SFS) register. Source FIFO is 16-entries deep.	00000	Source FIFO is full.
		00001	Source FIFO has one location free.
		00010	Source FIFO has two locations free.
		00011	Source FIFO has three locations free.
		00100	Source FIFO has four locations free.
		00101	Source FIFO has five locations free.
		00110	Source FIFO has six locations free.
		00111	Source FIFO has seven locations free.
		01000	Source FIFO has eight locations free.
		01001	Source FIFO has nine locations free.
		01010	Source FIFO has ten locations free.
		01011	Source FIFO has eleven locations free.
		01100	Source FIFO has twelve locations free.
		01101	Source FIFO has thirteen locations free.
		01110	Source FIFO has fourteen locations free.
		01111	Source FIFO has fifteen locations free.
		10000	Source FIFO is empty.
15:13	Reserved		
16	Graphic engine busy.	0	Graphic engine is idle.
		1	Graphics engine is busy. This is set as long as the command FIFO associated with the graphics engine has any command remaining. This signal is provided by the graphics engine.
31:17	Reserved.		

Register 4-11: GPIO Control Register 0 (CC02R: Index 08h, Offset 008h)

Bit	Bit Definition	Bit Value	Value Definition
0	Input control for GPIO 0	0	Disable input mode for GPIO 0
		1	Enable input mode for GPIO 0. The state of this pin is latched at the trailing edge of the power-on reset pulse. The latched value is used as mode-select pin 0.
1	Output control for GPIO 0	0	Disable output mode for GPIO. This is the default value for the bit.
		1	Enable output mode for GPIO.
2	Output data source select for the GPIO 0 pin when output mode is enabled.	0	CC02R[3] drives the GPIO 0 pin data value.
		1	A selected internal signal drives the GPIO 0 pin data value. This setting is only used for test mode.
3	Data value for the GPIO 0 pin. The value written into this bit is driven to the GPIO 0 pin if output mode is enabled for GPIO 0. When this bit is read, it reflects the value of the signal driven by the GPIO 0 pin if the input mode for GPIO 0 is enabled.		
4	GPIO 1 input control.	0	Disable input mode for GPIO 1.
		1	Enable input mode for GPIO 1. The state of this pin is latched at the trailing edge of the power-on reset pulse. The latched value is used as mode-select pin 1.
5	Output control for GPIO 1.	0	Disable output mode for GPIO 1. This is the bit's default value.
		1	Enable output mode for GPIO 1 pin.
6	Output data source select for the GPIO 1 pin when output mode is enabled.	0	CC02R[7] drives the GPIO 1 pin data value.
		1	A selected internal signal drives the GPIO 1 pin data value. This setting is only used for test mode.
7	Data value for the GPIO 1 pin. The value written into this bit is driven to the GPIO 1 pin if the output mode is enabled for GPIO 1. When this bit is read, it reflects the value of the signal driven by the GPIO 1 pin if the input mode for GPIO 1 is enabled.		
8	Input control for GPIO 2.	0	Disable input mode for GPIO 2.
		1	Enable input mode for GPIO 2. This is the default value for this bit. The state of this pin is latched at the trailing edge of the power-on reset pulse. The latched value is used as mode-select pin 2.
9	Output control for GPIO 2.	0	Disable output mode for GPIO 2. This is the default value for the bit.
		1	Enable output mode for GPIO 2.
10	Output data source select for the GPIO 2 pin when output mode is enabled.	0	CC02R[11] drives the GPIO 2 pin data value.
		1	A selected internal signal drives the GPIO 2 pin data value. This setting is only used for test mode.
11	Data value for the GPIO 2 pin. The value written into this bit is driven to the GPIO 2 pin if output mode is enabled for GPIO 2. When this bit is read, it reflects the value of the signal driven by the GPIO 2 pin if the input mode for GPIO 2 is enabled.		

Register 4-11: GPIO Control Register 0 (CC02R: Index 08h, Offset 008h)

Bit	Bit Definition	Bit Value	Value Definition
12	GPIO 3 input control.	0	Disable input mode for GPIO 3 pin.
		1	Enable input mode for GPIO 3. This is the default value for this bit. The state of this pin is latched at the trailing edge of the power-on reset pulse. The latched value is used a mode PWDN# pin enabler.
13	Output control for GPIO3.	0	Disable output mode for GPIO 3. This is the bit's default value.
		1	Enable output mode for the GPIO 3 pin.
14	Output data source select for GPIO 3 when output mode is enabled.	0	CC02R[15] drives the GPIO 3 pin data value.
		1	A selected internal signal drives the GPIO 3 pin data value. This setting is only used for test mode.
15	Data value for GPIO 3. The value written into this bit is driven to GPIO 3 pin if output mode is enabled for GPIO 3. When this bit is read, it reflects the value of the signal driven by the GPIO 3 pin if the input mode for GPIO 3 is enabled.		
16	GPIO 4 input control	0	Disable input mode for GPIO 4
		1	Enable input mode for GPIO 4. This is the default value for this bit. If the PWDN# pin is enabled, the GPIO 4 pin is used as the PWDN# pin, not as a GPIO pin.
17	Output control for GPIO 4	0	Disable output mode for GPIO 4. This is the bit's default value.
		1	Enable output mode for GPIO 4. This setting is not available if the PWDN# pin is enabled.
18	Output data source select for GPIO 4 when output mode is enabled.	0	CC02R[19] drives the GPIO 4 pin data value.
		1	A selected internal signal drives the GPIO 4 pin data value. This setting is only used for test mode.
19	Data value for the GPIO 4. The value written into this bit is driven to GPIO 4 pin if output mode is enabled for GPIO 4. When this bit is read, it reflects the value of the signal driven by the GPIO 4 pin if the input mode for GPIO 4 is enabled.		
20	Input control for the GPIO 5 pin. ***Note:*** *MQ-1132 only*	0	Disable input mode for GPIO5.
		1	Enable input mode for the GPIO 5 pin. This is the default value for this bit.
21	Output control for the GPIO 5 pin. ***Note:*** *MQ-1132 only*	0	Disable output mode for GPIO 5. This is the default value for the bit.
		1	Enable output mode for GPIO 5.
22	Output data source select for the GPIO 5 when output mode is enabled. ***Note:*** *MQ-1132 only*	0	CC02R[23] drives the GPIO 5 pin data value.
		1	A selected internal signal drives the GPIO 5 pin data value. This setting is only used for test mode.
23	Data value for the GPIO 5 pin. The value written into this bit is driven to GPIO 5 pin if output mode is enabled for GPIO 5. When this bit is read, it reflects the value of the signal driven by the GPIO 5 pin if the input mode for GPIO 5 is enabled. ***Note:*** *MQ-1132 only*		

Register 4-11: GPIO Control Register 0 (CC02R: Index 08h, Offset 008h)

Bit	Bit Definition	Bit Value	Value Definition
24	Input control for the CKIO pin when used as a GPIO pin.	0	Disable input mode for CKIO. This is the default value for this bit.
		1	Enable input mode for CKIO.
25	Output control for the CKIO pin when used as a GPIO pin.	0	Disable output mode for CKIO. This is the default value for the bit.
		1	Enable output mode for CKIO.
26	Output data source select for the CKIO pin when used as a GPIO pin.	0	CC02R[27] drives the CKIO pin data value.
		1	A selected internal signal drives the CKIO pin data value. This setting is only used for test mode.
27	Data value for the CKIO pin when used as GPIO 6. The value written into this bit is driven to CKIO pin if output mode is enabled for CKIO. When this bit is read, it reflects the value of the signal driven by the CKIO pin if the input mode for CKIO when used as GPIO 6.		
28	Input control for the BS# pin.	0	Disable input mode for BS#. This is the default value for the bit.
		1	Enable input mode for the BS#. This is the default value for this bit.
29	Output control for the BS# pin when it is used as GPIO 7.	0	Disable output mode for the BS# pin. This is the default value for the bit.
		1	Enable output mode for BS#.
30	Output data source select when it is used as GPIO 7.	0	CC02R[27] drives the BS# pin data value.
		1	A selected internal signal drives the BS# pin data value. This setting is only used for test mode.
31	Data value for the BS# pin when it's used as GPIO-7. The value written into this bit is driven to the BS# pin if output mode is enabled for BS#. When this bit is read, it reflects the value of the signal driven by the BS# pin if the input mode for BS# pin when used as GPIO 7.		

Register 4-12: GPIO Control Register 1 (CC03R: Index 0Ch, Offset 00Ch)

Bit	Bit Definition	Bit Value	Value Definition
5:0	Reserved. Must be programmed to 0.		
8	Input control for GPIO 20 pin ***Note:*** *MQ-1132 only*	0	Disable input mode for GPIO 20.
		1	Enable input mode for GPIO 20. This is the default value for this bit.
9	Output control for GPIO 20 pin. ***Note:*** *MQ-1132 only*	0	Disable output mode for the GPIO 20 pin. This is the default value for the bit.
		1	Enable output mode for GPIO 20.
10	Output data source select for the GPIO 20 pin when output mode is enabled. ***Note:*** *MQ-1132 only*	0	CC03R[11] drives the GPIO 20 pin data value.
		1	A selected internal signal drives the GPIO 20 pin data value. This setting is only used for test mode.
11	Data value for the GPIO 20 pin. The value written into this bit is driven to the GPIO 20 pin if output mode is enabled for GPIO 20. When this bit is read, it reflects the value of the signal driven by GPIO 20 pin if the input mode for GPIO 20 is enabled. ***Note:*** *MQ-1132 only*		
12	GPIO 21 pin input control. ***Note:*** *MQ-1132 only*	0	Disable input mode for GPIO 21.
		1	Enable input mode for GPIO 21. This is the default value for this bit.
13	Output control for GPIO 21 pin. ***Note:*** *MQ-1132 only*	0	Disable output mode for GPIO 21. This is the bit's default value.
		1	Enable output mode for GPIO 21.
14	Output data source select for GPIO 21 when output mode is enabled. ***Note:*** *MQ-1132 only*	0	CC03R[15] drives the GPIO 21 pin data value.
		1	A selected internal signal drives the GPIO 21 pin data value. This setting is only used for test mode.
15	Data value for the GPIO 21 pin. The value written into this bit is driven to the GPIO 21 pin if output mode is enabled for GPIO 21. When this bit is read, it reflects the value of the signal driven by GPIO 21 pin if the input mode for GPIO 21 is enabled. ***Note:*** *MQ-1132 only*		
16	GPIO 22 pin input control. ***Note:*** *MQ-1132 only*	0	Disable input mode for GPIO 22.
		1	Enable input mode for GPIO 22. This is the default value for this bit.
17	Output control for GPIO 22 pin. ***Note:*** *MQ-1132 only*	0	Disable output mode for GPIO 22. This is the bit's default value.
		1	Enable output mode for GPIO 22.
18	Output data source select for the GPIO 22 pin when output mode is enabled. ***Note:*** *MQ-1132 only*	0	CC03R[19] drives the GPIO 22 pin data value.
		1	A selected internal signal drives the GPIO 22 pin data value. This setting is only used for test mode.

Register 4-12: GPIO Control Register 1 (CC03R: Index 0Ch, Offset 00Ch)

Bit	Bit Definition	Bit Value	Value Definition
19	Data value for the GPIO 22 pin. The value written into this bit is driven to the GPIO 22 pin if output mode is enabled for GPIO 22. When this bit is read, it reflects the value of the signal driven by GPIO 22 pin if the input mode for GPIO 22 pin is enabled. ***Note:*** *MQ-1132 only*		
20	Input control for the GPIO 23 pin. ***Note:*** *MQ-1132 only*	0	Disable input mode for GPIO 23.
		1	Enable input mode for GPIO 23. This is the default value for this bit.
21	Output control for the GPIO 23 pin. ***Note:*** *MQ-1132 only*	0	Disable output mode for GPIO 23. This is the default value for the bit.
		1	Enable output mode for GPIO 23.
22	Output data source select for the GPIO 23 pin when output mode is enabled. ***Note:*** *MQ-1132 only*	0	CC03R[23] drives the GPIO 23 pin data value.
		1	A selected internal signal drives the GPIO 23 pin data value. This setting is only used for test mode.
23	Data value for the GPIO 23 pin. The value written into this bit is driven to the GPIO 23 pin if output mode is enabled for GPIO 23. When this bit is read, it reflects the value of the signal driven by the GPIO 23 pin if the input mode for GPIO 23 is enabled. ***Note:*** *MQ-1132 only*		
24	Input control for GPIO 24. ***Note:*** *MQ-1132 only*	0	Disable input mode for GPIO 24.
		1	Enable input mode for GPIO 24. This is the default value for this bit.
25	Output control for the GPIO 23 pin. ***Note:*** *MQ-1132 only*	0	Disable output mode for GPIO 24. This is the default value for the bit.
		1	Enable output mode for GPIO 24.
26	Output data source select for the GPIO 24 pin when output mode is enabled. **Note:** MQ-1132 only	0	CC03R[27] drives the GPIO 24 pin data value.
		1	A selected internal signal drives the GPIO 24 pin data value. This setting is only used for test mode.
27	Data value for the GPIO 24 pin. The value written into this bit is driven to the GPIO 24 pin if output mode is enabled for GPIO 24. This bit reflects the value of the signal driven by the GPIO 24 pin if the input mode for GPIO 24 is enabled. **Note:** MQ-1132 only		
28	Input control for GPIO 25. **Note:** MQ-1132 only	0	Disable input mode for GPIO 25.
		1	Enable input mode for GPIO 25. This is the default value for this bit.
29	Output control for GPIO 25. **Note:** MQ-1132 only	0	Disable output mode for GPIO 25. This is the default value for the bit.
		1	Enable output mode for the GPIO 25 pin.

Register 4-12: GPIO Control Register 1 (CC03R: Index 0Ch, Offset 00Ch)

Bit	Bit Definition	Bit Value	Value Definition
30	Output data source select for the GPIO 25 pin when output mode is enabled. **Note:** MQ-1132 only	0	CC03R[31] drives the GPIO 25 pin data value.
		1	A selected internal signal drives the GPIO 25 pin data value. This setting is only used for test mode.
31	Data value for the GPIO 25 pin. The value written into this bit is driven to the GPIO 25 pin if output mode is enabled for GPIO 25. When this bit is read, it reflects the value of the signal driven by the GPIO 25 pin if the input mode for GPIO 25 is enabled. **Note:** MQ-1132 only		

Register 4-13: CPU Test Mode Register 0 (CC04R: Index 10h, Offset 010h)

Bit	Bit Definition	Bit Value	Value Definition
31:0	CPU test mode enable bits (factory test mode)		

4.6 Interrupt Controller

The interrupt controller is part of the CPU interface. The interrupt controller is designed with an assumption that only one interrupt is available for MQ-1100/1132. By default this signal is an active low signal. However, this signal can be programmed to be either active low or active high.

The Interrupt Status Register bits, IN02R[13:0], indicate the status of the interrupts generated by the bus interface module. These bits are set whenever the corresponding interrupt occurs while not masked by one of the associated Interrupt Mask Register bits IN01R[13:0]. Once set, the Interrupt Status Register bits retain their values until cleared by the CPU by writing a "1" to the bit of IN02R[13:0] that is to be cleared.

Interrupt Status Register bits IN02R[19:14] indicate the status of the interrupts generated by the various peripheral modules; SPI, I2S and USB (except for USB host controller global-suspend mode interrupt status which is bit 13 of IN02R). The setting and resetting of these bits is controlled by the corresponding peripheral module. They are set whenever the corresponding interrupt occurs while not masked by one of the associated Interrupt Mask Register bits, IN01R[19:14]. Once set, these Interrupt Status Register bits retain their values until they are cleared by the CPU by writing a "1" to the corresponding peripheral interrupt status register bits.

The Interrupt Mask Register (IN01R) bits [13:0] control both the generation of the corresponding Interrupt Status Register bits and the generation of the external interrupt when the Interrupt Enable bit IN00R[0] is set. The Interrupt Mask Register bits [19:14] only control the generation of the external interrupt when the Interrupt Enable bit 1N00R[0] is set.

4.6.1. Interrupt Controller Registers

Table 4-4 specifies the index, offset and reset values for the interrupt controller registers.

TABLE 4-4: Interrupt Controller Register Index and Reset Values

Register	Index	Offset	Reset Value	See Description
IN00R	00h	100h	0000-0000h	*Register 4-14 on page 79*
IN01R	04h	104h	0000-0000h	*Register 4-15 on page 80*
IN02R	08h	108h	0000-0000h	*Register 4-16 on page 81*
IN03R	0Ch	10Ch	0000-0000h	*Register 4-17 on page 82*

Register 4-14 through *Register 4-17* specify the interrupt control register bit values and definitions.

Register 4-14: Global Interrupt Control Register (IN00R: Index 00h, Offset 100h)

Bit	Bit Definition	Bit Value	Value Definition
0	Interrupt enable bit.	0	Disable the MQ-1100/1132 to the CPU.
		1	Enable the MQ-1100/1132 to the CPU.
1	Polarity of the interrupt pin.	0	Interrupt is active low.
		1	Interrupt is active high.
2	GPIO interrupt polarity – GPIO 0 – level triggered interrupt.	0	Interrupt occurs when GPIO 0 is at level 0.
		1	Interrupt occurs when GPIO 0 is at level 1.
3	GPIO interrupt polarity – GPIO 1 – level triggered interrupt.	0	Interrupt occurs when GPIO 1 is at level 0.
		1	Interrupt occurs when GPIO 1 is at level 1
4	GPIO interrupt polarity – GPIO 2 – level triggered interrupt.	0	Interrupt occurs when GPIO 2 is at level 0.
		1	Interrupt occurs when GPIO 2 is at level 1.
31:5	Reserved		

Register 4-15: Interrupt Mask Register (IN01R: Index 04h, Offset 104h)

Bit	Bit Definition	Bit Value	Value Definition
0	Graphics controller – vertical synchronization enable – rising edge mask.	0	Interrupt is masked.
		1	Interrupt is not masked.
1	Graphics controller – vertical synchronization enable – falling edge mask.	0	Interrupt is masked.
		1	Interrupt is not masked.
2	Graphics controller – vertical display enable – rising edge mask.	0	Interrupt is masked.
		1	Interrupt is not masked.
3	Graphics controller – vertical display enable – falling edge mask.	0	Interrupt is masked.
		1	Interrupt is not masked.
4	Bus-cycle abort interrupt mask.	0	Interrupt is masked.
		1	Interrupt is not masked.
5	GPIO pin 0 – interrupt mask.	0	Interrupt is masked.
		1	Interrupt is not masked.
6	GPIO pin 1 – interrupt mask.	0	Interrupt is masked.
		1	Interrupt is not masked.
7	GPIO pin 2 – interrupt mask.	0	Interrupt is masked.
		1	Interrupt is not masked.
8	Command FIFO half empty mask.	0	Interrupt is masked.
		1	Interrupt is not masked.
9	Command FIFO empty mask.	0	Interrupt is masked.
		1	Interrupt is not masked.
10	Source FIFO half empty mask.	0	Interrupt is masked.
		1	Interrupt is not masked.
11	Source FIFO empty mask.	0	Interrupt is masked.
		1	Interrupt is not masked.
12	Graphics engine is idle mask.	0	Interrupt is masked.
		1	Interrupt is not masked.
13	USB host controller global-suspend mode interrupt mask. ***Note:*** *MQ-1132 only*	0	Interrupt is masked.
		1	Interrupt is not masked.
14	USB host controller remote wake-up interrupt mask. [1] ***Note:*** *MQ-1132 only*	0	Interrupt is masked.
		1	Interrupt is not masked.
15	USB host controller interrupt mask. [2] ***Note:*** *MQ-1132 only*	0	Interrupt is masked.
		1	Interrupt is not masked.
16	USB device – interrupt mask.	0	Interrupt is masked.
		1	Interrupt is not masked.
17	I^2S interrupt mask. ***Note:*** *MQ-1132 only*	0	Interrupt is masked.
		1	Interrupt is not masked.
18	SPI interrupt mask. ***Note:*** *MQ-1132 only*	0	Interrupt is masked
		1	Interrupt is not masked.
19	USB device wake-up interrupt mask.	0	Interrupt is masked.
		1	Interrupt is not masked.
31:17	Reserved		

1. This is only valid if the oscillator clock or USB host clock is disabled.
2. This is only valid for interrupts specified in the OHCI interrupt-status register.

Register 4-16: Interrupt Status Register (IN02R: Index 08h, Offset 108h)

Bit	Bit Definition	Bit Value	Value Definition
0	Graphics controller – vertical synchronization enable – rising edge.	0	Interrupt event is false.
		1	Interrupt event is true.
1	Graphics controller – vertical synchronization enable – falling edge.	0	Interrupt event is false.
		1	Interrupt event is true.
2	Graphics controller – vertical display enable – rising edge.	0	Interrupt event is false.
		1	Interrupt event is true.
3	Graphics controller – vertical display enable – falling edge.	0	Interrupt event is false.
		1	Interrupt event is true.
4	Bus cycle abort interrupt status.	0	Interrupt event is false.
		1	Interrupt event is true.
5	GPIO 0 – interrupt status.	0	Interrupt event is false.
		1	Interrupt event is true.
6	GPIO 1 – interrupt status.	0	Interrupt event is false.
		1	Interrupt event is true.
7	GPIO 2 – interrupt status.	0	Interrupt event is false.
		1	Interrupt event is true.
8	Command FIFO half empty.	0	Interrupt event is false.
		1	Interrupt event is true.
9	Command FIFO empty.	0	Interrupt event is false.
		1	Interrupt event is true.
10	Source FIFO half empty.	0	Interrupt event is false.
		1	Interrupt event is true.
11	Source FIFO empty.	0	Interrupt event is false.
		1	Interrupt event is true.
12	Graphics engine is idle	0	Interrupt event is false.
		1	Interrupt event is true.
13	USB host controller global-suspend mode interrupt status (MQ-1132 only)	0	Interrupt event is false.
		1	Interrupt event is true.
14	USB host controller remote wake-up interrupt status. (MQ-1132 only)	0	Interrupt event is false.
		1	Interrupt event is true.
15	USB host controller OHCI interrupt status. (MQ-1132 only)	0	Interrupt event is false.
		1	Interrupt event is true.
16	USB device interrupt	0	Interrupt event is false.
		1	Interrupt event is true.
17	I^2S interrupt status. (MQ-1132 only)	0	Interrupt event is false.
		1	Interrupt event is true.
18	SPI interrupt status. (MQ-1132 only)	0	Interrupt event is false.
		1	Interrupt event is true.
19	USB device wake-up interrupt status.	0	Interrupt event is false.
		1	Interrupt event is true.
31:20	Reserved.		

Register 4-17: Interrupt Pin Raw Status Register (IN03R: Index 0CH, Offset 10Ch)

Bit	Bit Definition	Bit Value	Value Definition
0	Graphics Controller – Vertical Sync Enable	0	Interrupt event is false.
		1	Interrupt event is true.
1	Graphics Controller – Vertical Display Enable	0	Interrupt event is false.
		1	Interrupt event is true.
2	SCC Raw-Interrupt Status	0	Interrupt event is false.
		1	Interrupt event is true.
3	SPI Raw-Interrupt Status	0	Interrupt event is false.
		1	Interrupt event is true.
4	GPIO Pin 0	0	Interrupt event is false.
		1	Interrupt event is true.
5	GPIO Pin 1	0	Interrupt event is false.
		1	Interrupt event is true.
6	GPIO Pin 2	0	Interrupt event is false.
		1	Interrupt event is true.
7	Reserved	0	Interrupt event is false.
		1	Interrupt event is true.
8	Graphics Engine Busy Signal	0	Interrupt event is false.
		1	Interrupt event is true.
9	Source FIFO Empty	0	Interrupt event is false.
		1	Interrupt event is true.
10	Source FIFO Half Empty	0	Interrupt event is false.
		1	Interrupt event is true.
11	Command FIFO Empty	0	Interrupt event is false.
		1	Interrupt event is true.
12	Command FIFO Half Empty	0	Interrupt event is false.
		1	Interrupt event is true.
13	USB Host Controller OHCI specific Raw-Interrupt Status (MQ-1132 only)	0	Interrupt event is false.
		1	Interrupt event is true.
14	USB Host Global-Suspend Raw Interrupt Status (MQ-1132 only)	0	Interrupt event is false.
		1	Interrupt event is true.
15	USB Host Remote Wakeup Raw Interrupt Status (MQ-1132 only)	0	Interrupt event is false.
		1	Interrupt event is true.
16	USB Device Raw-Interrupt Status	0	Interrupt event is false.
		1	Interrupt event is true.
17	USB Device wakeup Raw-Interrupt Status	0	Interrupt event is false.
		1	Interrupt event is true.
31:18	Reserved		

4.7 PCI Registers

The MQ-1132, is a PCI compliant device, it implements the specific record structure on the 256-byte configuration space. The configuration space is divided into a predefined header region and a device dependent region. The MQ-1132 implements only the necessary and relevant registers. This space is accessible at all times.

Figure 4-3 illustrates the registers in the configuration space.

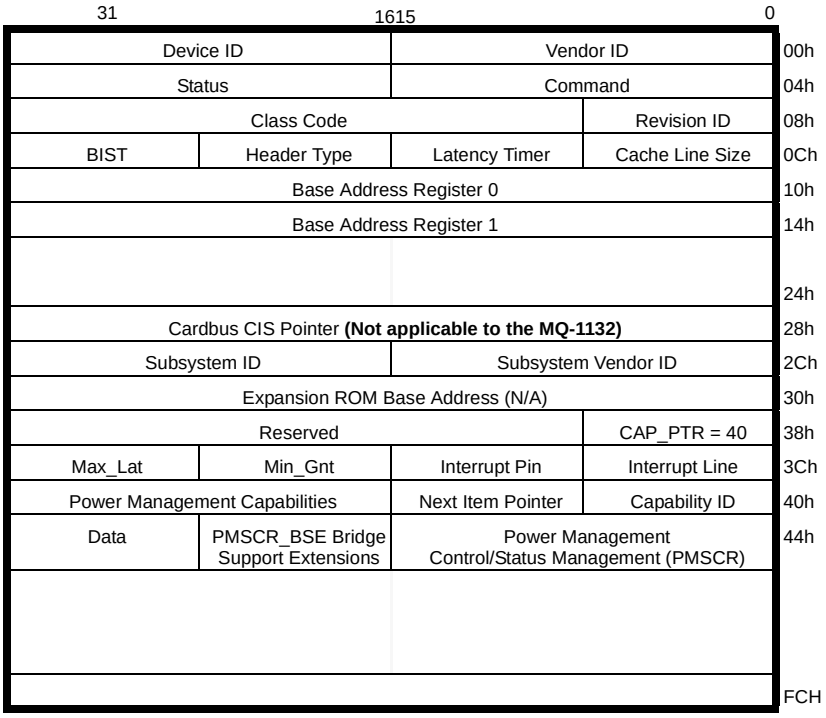


Figure 4-3. Standard PCI Configuration Space Header Type 00h

The MQ-1132 device completely conforms with placing the data structure in the same format as proposed by a Type 00h Configuration Space Header associated with the PCI 2.1 Specification.

Table 4-5 includes the index, offset and reset values for the Configuration Space registers.

TABLE 4-5: Index of Configuration Space Registers

Register	Index	Offset	Reset Value	See Description
PC00R	00h	400h	0120-4D51(hex)	*Register 4-18 on page 84*
PC01R	04h	404h	0280-0000(hex)	*Register 4-19 on page 84*
PC02R	08h	408h	0380-0000 (hex)	*Register 4-20 on page 85*
PC03R	0Ch	40Ch	0000-0000(hex)	*Register 4-21 on page 85*
PC04R	10h	410h	—	*Register 4-22 on page 85*
PC05R	14h	414h	—	*Register 4-23 on page 86*
PC0BR	2Ch	42Ch	0000-0100(hex)	*Register 4-25 on page 86*
PC0FR	3Ch	43Ch	0000-0100(hex)	*Register 4-24 on page 86*

4.7.1. Registers in the Configuration Space

Register 4-18: Device ID / Vendor ID Register (PC00R: Index 00h, Offset 400h)

PC00R	**Device ID / Vendor ID Register** Index: 00h in Configuration Space Reset value: 0120-4D51(hex) This register specifies the Vendor ID and the Device ID **Vendor ID (Read only)** These bits are set to 4D51(hex) (ASCII value of "MQ").

Register 4-19: Command/Status Register (PC01R: Index 04h, Offset 404h)

PC01R	**Command/Status Register** Index: 04h in Configuration space	Reset value: 0280-0000(hex)
15-0	**Command Register (Read/Write)**	
	0	IO Space Control - MQ-1132 does not respond to IO accesses. This bit is not used by the MQ-1132 and should be set to a '0'.
	1	Memory Space Control - After reset, this bit is reset to '0'. To enable the memory access, this bit has to be set to a '1'.
	2	Bus Master Control - This bit is not used by the MQ-1132 and should be set to a '0'.
	3	Special Cycle - This bit is not used by the MQ-1132 and should be set to a '0'.
	4	Memory Write and Invalidate - This bit is not used by the MQ-1132 and should be set to a '0'
	5	VGA Palette Snoop - This bit is not used by the MQ-1132 and should be set to a '0'.
	6	Parity Error Checking Enable - If this bit is set to a '1', the MQ-1132 shall report an error if a parity error occurs. After reset its value is set to a '0'.
	7	Address/Data Stepping - This bit is not used by the MQ-1132 and should be set to a '0'.
	8	SERR# Enable - If it is set to a '1', it enables the SERR# drive; otherwise, it disable the SERR# driver. After reset its value is set to a '0'.
	15-9	Reserved
31-16	Status Register	
	20-16	Reserved.
	21	66 MHz Capability - MQ-1132 supports 33 MHz clock; therefore, this bit is set to a '0'.
	22	User Definable Features Supported: this bit is set to a '0'.
	23	Fast Back-to-Back Capability: MQ-1132 supports the Fast Back-to-Back transfer. This bit is set to a '1'.
	24	Reserved.
	26-25	DEVSEL Timing: MQ-1132 supports medium timing. The value is set to "01".
	27	Signaled Target Abort: this bit is set to a '0'.
	29-28	Reserved.
	30	SERR# Assertion - MQ-1132 sets this bit to a '1' when it asserts the SERR#. After reset, its value is a '0'. Software needs to write a '1' to this bit to clear it.
	31	Parity Error Detect - MQ-1132 sets this bit to a '1' when it detects a parity error. Software needs to write a '1' to this bit to clear it.

Register 4-20: Class Code / Revision ID (PC02R: Index 08h, Offset 408h)

PC02R	Class Code / Revision ID	
	Index: 08h in Configuration space Reset value: 0380-0000 (hex) The register specifies the revision and Class Code.	
	7-0	Revision ID (Read Only): This field reflects the revision of the chip.
	15-8	Programming Interface Code: This field contains a "00" (hex). This value in conjunction with the Base Class Code being "03" (hex) and the Programming Interface Code being "00" (hex) implies that the Display Controller is classified under the "Other Display Controller" Category.
	23-16	Sub-Class Code: This field contains a "80" (hex). This value in conjunction with the Base Class Code being "03" (hex) and the Programming Interface Code being "00" (hex) implies that the Display Controller is classified under the "Other Display Controller" Category.
	31-24	Base Class Code: (Read Only). The value of this field is a "03" (hex) that implies the MQ-1132 is a Display Controller.

Register 4-21: Cache Line Size/Latency Timer/Header Type/BIST Register (PC03R: Index 0Ch, Offset 40Ch)

PC03R	Cache Line Size/Latency Timer/Header Type/BIST Register	
	Index: 0Ch in Configuration space Reset value: 0000-0000(hex)	
	7-0	Cache Line Size (Read Only): MQ-1132 does not use this field. The bits are set to a "00" (hex).
	15-8	Latency Timer (Ready Only): MQ-1132 does not use this field. The bits are set to a "00" (hex).
	23-16	Header Type - The bits are set to a "00" (hex) to indicate that the Configuration Space is of Header Type 0.
	31-24	BIST (Ready Only): MQ-1132 does not use this field. The bits are set to a "00" (hex).

Register 4-22: Base Address Register 0 (PC04R: Index 10h, Offset 410h)

PC04R	Base Address Register 0	
	Index: 10Ch in Configuration space The register specifies the Base Address for the register space.	
	0	Memory Space Indicator. This bit is set to a '0' that implies the MQ-1132's registers are mapped into the Memory Space.
	2-1	Type: the bits are set to a "00" that implies the MQ-1132 is located anywhere in the 32-bit address space.
	3	Prefetchable (Read Only): this bit is set to a '0'.
	21-4	Memory Space Range (Read Only): The bits are set to all 0s to specify the address range of 512 Kbyte that the MQ-1132 needs.
	31-22	Base Address 0 (Read/Write): Base Address 0.

Register 4-23: Base Address Register 1 (PC05R: Index 14h, Offset 414h)

PC05R	Base Address Register 1	
	Index: 14h in Configuration space The register specifies the Base Address for the frame buffer (memory) space.	
	0	Memory Space Indicator: this bit is set to '0', indicating the MQ-1132 registers are mapped into the Memory Space.
	2-1	Type: the bits are set to a "00", indicating the MQ-1132 is located anywhere in the 32-bit address space.
	3	Prefetchable (Read Only): this bit is set to a '0'.
	21-4	Memory Space Range (Read Only): the bits are set to all 0s to specify the address range of 4 Kbyte that the MQ-1132 needs.
	31-22	Base Address 1 (Read/Write): Base Address 1

Register 4-24: System Vendor ID / Subsystem ID (PC0BR: Index 2Ch, Offset 42Ch)

PC0BR	Interrupt Line/Interrupt Pin/Min_Lat Register	
	Index: 2Ch in Configuration space Reset value: 0000-0100(hex) The register specifies the Subsystem Vendor ID / Subsystem ID.	
	15-0	Subsystem Vendor ID (Read/Write): this field contains the value of the Subsystem Vendor ID that is initialized by the system software.
	31-16	Subsystem ID (Read/Write): this field contains the value of the Subsystem Vendor ID that is initialized by the system software.

Register 4-25: Interrupt Line/Interrupt Pin/Min_Lat Register (PC0FR: Index 3Ch, Offset 43Ch)

PC0FR	Interrupt Line/Interrupt Pin/Min_Lat Register	
	Index: 3Ch in Configuration space Reset value: 0000-0100(hex) The register specifies the Interrupt Line, Interrupt Pin, Minimum Grant time, and the Maximum Latency values.	
	7-0	Interrupt Line (Read/Write): This field contains the interrupt line routing information that is initialized by the system software.
	15-8	Interrupt Pin (Read Only): the bits are set to a "01" hex to implies that the MQ-1132's interrupt is routed to INTA# of the PCI bus.
	31-16	Minimum Grant / Maximum Latency (Read Only): the bits are set to a "0000" hex to implies that the MQ-1132 does not have a major requirement for the settings of latency timers.

4.8 Memory Interface Unit

The MIU consists of an arbiter, sequencer, register block, display refresh controller, graphics engine source-read controller, graphics engine destination read controller, graphics engine destination write controller, USB host-memory controller, memory-clock controller, display, CPU, and graphics engine FIFO blocks. All the memory requests for the arbiter are generated in the MIU.

The memory interface module supports the following features:

- 256-Kbyte SRAM
- Request serving with programmable corresponding burst count
- Separate read and write 64-bit buses

TABLE 4-6: MIU Register Index and Reset Values

Register	Index	Offset	Reset Value	See Description
MM00R	00h	080h	xxxx-xxx0h	*Register 4-26 on page 87*
MM01R	04h	084h	xxxx-xxx0h	*Register 4-27 on page 87*
MM02R	08h	088h	xxxx-xxx0h	*Register 4-28 on page 89*
MM03R	0Ch	08Ch	xxxx-xxxh	*Register 4-29 on page 89*
MM04R	10h	090H	xxxx-xxxh	*Register 4-30 on page 89*

Register 4-26: MIU Interface Control 1 (MM00R: Index 00h, Offset 080h)

Bit	Bit Definition	Bit Value	Value Definition
0	MIU enable bit. Setting this bit enables the MIU block.	0	Powers down the MIU (resets value). Disable the MIU clock and activates the MIU reset.
		1	Enable the MIU.
1	MIU reset-enable bit. This register bit resets the MIU asynchronously.	0	Disable the MIU reset (resets value).
		1	Enable the MIU reset.
31:2	Reserved		

Register 4-27: MIU Interface Control 2 (MM01R: Index 04h, Offset 084h)

Bit	Bit Definition	Bit Value	Value Definition
0	Memory clock source. This bit specifies the clock source for the memory-interface clock.	0	48-MHz oscillator clock is used as memory clock source.
		1	Bus clock is used as memory clock source.
1	Reserved		
4:2	Memory interface clock divider. This parameter controls the clock divider for memory interface.	000	Clock divided by 1.
		001	Clock divided by 1.5.
		010	Clock divided by 2.
		011	Clock divided by 2.5.
		100	Clock divided by 3.
		101	Clock divided by 4.
		110	Clock divided by 5.
		111	Clock divided by 6.
6:5	Burst count for display refresh memory cycles. These bits control the size of the burst for the display refresh memory cycles in a memory page; if the MIU starts display refresh data fetching, it will fetch until it gets a burst count of 64 bits of data or it reaches the line end.	00	Burst size = 2
		01	Burst size = 4
		10	Burst size = 6
		11	Burst size = 8

Register 4-27: MIU Interface Control 2 (MM01R: Index 04h, Offset 084h)

Bit	Bit Definition	Bit Value	Value Definition
8:7	Burst count for graphics engine read and write memory cycles. These bits control the size of the burst for the graphics engine read/write memory cycles.	00	Burst size = 2
		01	Burst size = 4
		10	Burst size = 6
		11	Burst size = 8
10:9	Burst count for CPU write memory cycles. These bits control the size of the burst for the CPU write memory cycles.	00	Burst size = 2
		01	Burst size = 4
		10	Burst size = 6
		11	Burst size = 8
12:11	Burst count for I^2S read DMA. These bits control the size of the burst for the I^2S read memory cycles. (MQ-1132 only)	00	Burst size = 2
		01	Burst size = 4
		10	Burst size = 6
		11	Burst size = 8
14:13	Burst count for USB device DMA reads and writes. These bits control the size of the burst for USB device DMA-read and write memory cycles.	00	Burst size = 2
		01	Burst size = 4
		10	Burst size = 6
		11	Burst size = 8
19:16	GC1 display refresh FIFO threshold. Whenever the number of filled locations in GC1 display refresh FIFOs is less than this threshold, the memory request for GC1 is generated in order to fetch the display refresh data for GC1. Legal values are from 0001 to 1111.		
22:20	Graphics engine source read FIFO threshold. Whenever the number of filled locations in the graphics engine source read FIFO is less than this threshold, the memory request for the graphics engine source read is generated in order to fetch the source data for the graphics engine. Valid values are between 001 and 111.		
25:23	Graphics engine destination read FIFO threshold. Whenever the number of filled locations in the graphics engine destination read FIFO is less than this threshold, the memory request for the graphics engine source read is generated in order to fetch the source data for the graphics engine. Valid values are between 001 and 111.		
28:26	I^2S transmit FIFO threshold. Whenever the number of filled locations in I^2S transmit FIFO is less than this threshold, the memory request for I^2S read is generated in order to fetch the transmit data for I^2S. Legal values are from 001 to 111. (MQ-1132 only)		
31:29	Reserved		

Register 4-28: MIU Test Control Register 1 (MM02R: Index 08h, Offset 088h)

Bit	Bit Definition	Bit Value	Value Definition
0	MIU test mode enable. Only set this bit for test mode.	0	Disable MIU test mode.
		1	Enable MIU test mode.
3:1	GPIO source data select for MIU.		
31-4	Reserved		

Register 4-29: MIU Test Control 2 (MM03R: Index 0Ch, Offset 08Ch)

Bit	Bit Definition	Bit Value	Value Definition
15:0	Test control bits. (factory test mode)		Write 0 for normal operation.
31-16	Reserved		

Register 4-30: MIU Test Data Register (MM04R: Index 10h Offset 090h)

Bit	Bit Definition	Bit Value	Value Definition
31:0	Test data bits.(factory test mode)		Bit values are undefined for normal operation.

4.9 Graphics Controller

4.9.1. General Description and Architecture

This module consists of one graphics controller (GC) that can drive a display device. The GC can support one graphics image window (Window) and one hardware cursor (Cursor). A single 256 × 18-bit color palette is implemented for 1-, 2-, 4-, and 8-bpp modes.

The graphics controller module generates most of the necessary functions to refresh the display from the display frame buffer. These include:

- Generates the horizontal and vertical timing signals for the required display device.
- Generates horizontal and vertical timing signals for the graphics image window. Note that the graphics image resolution may be smaller than the display device resolution. Right and bottom side clipping of image window is implemented.
- Generates requests to memory controller to fetch image lines and controls data fetching from image FIFO. Pixel data serialization (1-, 2-, 4-, 8-, and 16-bpp) is performed and a single 256 × 18-bit color palette is implemented for 1-, 2-, 4-, and 8-bpp modes. Color palette is bypassed in 16-bpp mode.
- Generates horizontal and vertical timing signals for hardware cursor window. Hardware cursor is stored in the unused memory portion and one cursor line can be fetched at the beginning of display line. Hardware cursor data is then serialized and overlaid on top of graphics image window. Hardware cursor can be displayed anywhere within the display area. Hardware cursor offset and clipping at the right/bottom side of the display window can be performed. Hardware cursor is 2 bpp with a fixed 64 × 64 resolution. The hardware cursor bitmap format is compatible with Microsoft Windows cursor format. Windows cursor format is composed of an AND mask and a XOR mask:

AND	XOR	Result
0	0	Background Color
0	1	Foreground Color
1	0	Transparent
1	1	Inverted

- Performs dynamic power management to power down data paths outside the image window and hardware cursor areas.

The output of the graphics controller goes to the Flat Panel Interface (FPI) logic in 6-bit red, 6-bit green, 6-bit blue format or 8-bpp monochrome pixel format.

The graphics controller root clock (GRCLK) is generated from either the bus clock or from the oscillator clock. The graphics controller master clock (GMCLK) is derived from the root clock using a two-stage programmable clock divider.

Divisor 1 and Divisor 2 can be used together - along with a variety of root clock possibilities- to produce a wide variety of frequencies for the graphics controller.

Divisor 1 can be set from 1 to 6.5, in 0.5 increments. Divisor 2 can be set from 1 to 15, in integer increments. The root clock can be 48 MHz or less. Some common values are 48 MHz, 33 MHz, 18.432 MHz, 14.318 MHz and 12.288 MHz.

- Display image transformation:

  - Display image transformation is controlled by programming the line scanning direction (GC00R[13]), the y-direction scanning (GC0ER[15]) and the x-direction scanning (GC00R[12]) as shown in *Table 4-7* .

TABLE 4-7: Display Image Transformation

GC00R[13]	GC0ER[15]	GC00R[12]	Window Start Address Location	Mode
0	0	0	Top-left	Normal
0	0	1	Top-right	Flip Horizontally
0	1	0	Bottom-left	Flip Vertically
0	1	1	Bottom-right	180-degree rotation
1	0	0	Top-left	Flip on top-left bottom-right diagonal
1	0	1	Bottom-left	270-degree rotation
1	1	0	Top-right	90-degree rotation
1	1	1	Bottom-right	Swap XY with horizontal and vertical flip

The following diagram shows the possible display image transformations:

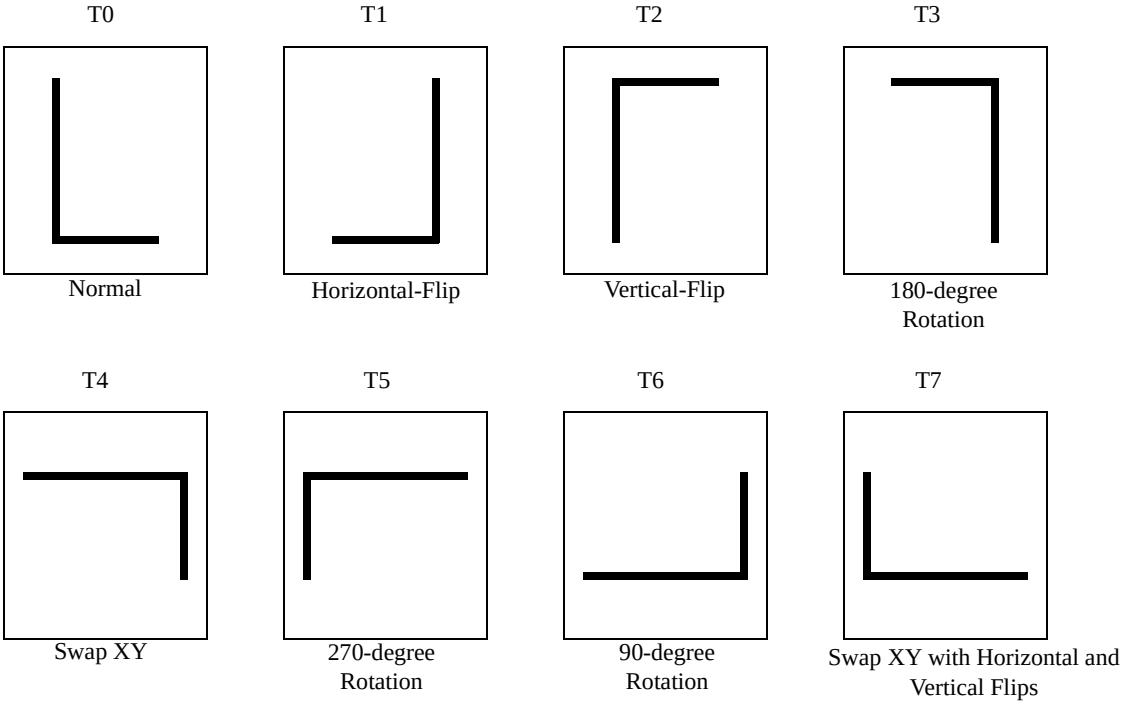


Figure 4-4. Display Transformation Modes

- Supports pixel doubling in both the horizontal and vertical directions via GC00R[15:14]. For instance, this can be used to fill a 320x320 display with only a 160x160 image in video memory.

The memory-size requirement for different graphics modes depends on color depth and window resolution. Additional memory is required for the hardware cursor. You must also allocate some memory space for built-in non-graphical peripheral DMA. *Table 4-8* specifies the memory requirement for graphics images.

TABLE 4-8: Graphics Controller Memory Requirements

Color Depth (bpp)	Memory Requirements (Bytes)				
	320 × 240	**320 × 320**	**640 × 240**	**640 × 480**	**800 × 600**
1	9,600	12,800	19,200	38,400	60,000
2	19,200	25,600	38,400	76,800	120,000
4	38,400	51,200	76,800	153,600	240,000
8	76,800	102,400	153,600		
16	153,600	204,800			

The memory requirements shown in *Table 4-8* is not dependent on display type. TFT LCD and single-scan STN (S-STN) displays do not require additional memory except for the hardware cursor.

If the hardware cursor is enabled, an additional 1,024 bytes are required for each cursor pattern requiring an alignment at 1 Kbyte boundary.

If more frame buffer memory is available after accounting for the graphics modes, hardware cursor, and DMA memory for other peripherals, then the remaining memory can be used by the display driver for caching purposes in order to increase performance.

Peak memory bandwidth requirement is:

pixel clock frequency × color depth (bpp8 for example).

Sustained memory bandwidth requirement is:

number of pixel per frame × color depth × refresh rate (frames per second).

4.9.2. Graphics Controller Register Definition

Table 4-9 specifies the index, offset and reset values for the Graphics Controller registers.

TABLE 4-9: Graphics Controller Register Index and Reset Values

Register	Index	Offset	Reset Value	See Description
GC00R	00h	180h	0000-0000h	*Register 4-31 on page 94*
GC01R	04h	184h	xxxx-xx00h	*Register 4-32 on page 96*
GC02R	08h	188h	xxxx-xxxh	*Register 4-33 on page 97*
GC03R	0Ch	18Ch	xxxx-xxxxh	*Register 4-34 on page 97*
GC04R	10h	190h	xxxx-xxxxh	*Register 4-35 on page 98*
GC05R	14h	194h	xxxx-xxxxh	*Register 4-36 on page 98*
GC06R	18h	198h	xxxx-0000h	*Register 4-37 on page 98*
GC07R	1Ch	19Ch	xxxx-0000h	*Register 4-38 on page 98*
GC08R	20h	1A0h	xxxx-xxxxh	*Register 4-39 on page 99*
GC09R	24h	1A4h	xxxx-xxxxh	*Register 4-40 on page 99*
GC0AR	28h	1A8h		*Register 4-41 on page 99*
GC0BR	2Ch	1ACh	xxxx-xxxxh	*Register 4-42 on page 100*
GC0CR	30h	1B0h	xxxx-xxxxh	*Register 4-43 on page 100*
GC0DR	34h	1B4h	xxxx-xxxxh	*Register 4-44 on page 100*
GC0ER	38h	1B8h	xxxx-xxxxh	*Register 4-45 on page 101*
GC0FR	3Ch	1BCh		*Register 4-46 on page 101*
GC10R	40h	1C0h	xxxx-xxxxh	*Register 4-47 on page 101*
GC11R	44h	1C4h	xxxx-xxxxh	*Register 4-48 on page 102*
GC12R	48h	1C8h	xxxx-xxxxh	*Register 4-49 on page 102*
GC13R	4Ch	1CCh	xxxx-xxxxh	*Register 4-50 on page 103*
GC14R	50h	1D0h		*Register 4-51 on page 103*
GC15R	54h	1D4h		*Register 4-52 on page 103*
GC16R	58h	1D8h		*Register 4-53 on page 103*
GC17R	5Ch	1DCh		*Register 4-54 on page 104*
GC18R	60h	1E0h		*Register 4-55 on page 105*
GC19R	64h	1E4h		*Register 4-56 on page 105*
GC1AR	68h	1E8h	xxxx-xxxxh	*Register 4-57 on page 105*
GC1BR	6Ch	1ECh	xxxx-xxxxh	*Register 4-58 on page 105*
GC1CR	70h	1F0h	xxxx-xxxxh	*Register 4-59 on page 109*
GC1DR	74h	1F4h	xxxx-xxxxh	*Register 4-60 on page 110*
GC1ER	78h	1F8h	xxxx-xxxxh	*Register 4-61 on page 112*
GC1FR	7Ch	1FCh	xxxx-xxxxh	*Register 4-62 on page 114*

Register 4-31 through *Register 4-58 on page 105* show the interrupt control register bit values and definitions.

Register 4-31: Graphics Controller Control Register (GC00R: Index 0h, Offset 180h)

Bit	Bit Definition	Bit Value	Value Definition
0	Setting this bit will enable the flat panel interface logic and graphic controller. If this bit is reset, the flat panel interface logic and the controller are powered down and reset.	0	Disable the graphics controller.
		1	Enable the graphics controller.
1	Horizontal counter reset. This bit performs the software reset on the horizontal counter.	0	Enable the horizontal counter.
		1	Resets and initializes the horizontal counter with the content of GC06R[10:0].
2	Vertical counter reset. This bit performs the software reset on the vertical counter.	0	Enable the vertical counter.
		1	Resets and initializes the vertical counter with the content of GC07R [9:0]
3	Image window enable. This bit enables the graphics image window.	0	Disable the image window.
		1	Enable the image window.
7:4	Graphics color depth (GCD). This parameter specifies the graphics image window's bpp when the main window buffer is selected.	0000	1-bpp graphics. Color palette is enabled.
		0001	2-bpp graphics. Color palette is enabled.
		0010	4-bpp graphics. Color palette is enabled.
		0011	8-bpp graphics. Color palette is enabled.
		0100	Reserved.
		0101	Reserved.
		0110	Reserved.
		0111	Reserved.
		1000	1-bpp monochrome graphics. Color palette is bypassed.
		1001	2-bpp monochrome graphics. Color palette is bypassed.
		1010	4-bpp monochrome graphics. Color palette is bypassed.
		1011	8-bpp monochrome graphics. Color palette is bypassed.
		1100	16-bpp (RGB565) graphics with color palette bypassed.
		1101	Reserved.
		1110	Reserved.
		1111	Reserved.
8	Hardware cursor enable. This bit enables the hardware cursor.	0	Disable hardware cursor.
		1	Enable hardware cursor.
9	Reserved. Must be programmed to 0	0	
11:10	Image window double buffer control. This bit is effective only when bit 3 is set. Double buffering is supported for the image window: the first buffer is the main window buffer, and the second buffer is the alternate window buffer. Power management logic can also be programmed to force the selection of the alternate window buffer in some power states.	00	Display main window buffer (alternate window buffer is not displayed). The window start address parameter is used in this mode.
		01	Double buffering is controlled by graphics engine (GE) module. At the end of a graphics command, the graphics engine module can be programmed to send control signals to the graphics controller to select the image window buffer to be displayed in the next frame.
		10	Alternate window buffer is displayed (main window buffer is not displayed). In this mode, the alternate window start address parameter is used.
		11	Reserved.

Register 4-31: Graphics Controller Control Register (GC00R: Index 0h, Offset 180h)

Bit	Bit Definition	Bit Value	Value Definition
12	X-direction scanning. Controls x-direction scanning. Y-direction scanning is controlled by programming the positive and negative stride value. Decrementing x-direction together with negative stride (decrementing y-direction) can be programmed for 180° image rotation. This bit affects both graphics image window and cursor horizontal scanning direction.	0	Scan in incrementing (positive) x-direction (left to right). This setting is used for 0° or 270° rotation.
		1	Scan in decrementing (negative) x-direction (right to left). This setting is used for 90° or 180° rotation.
13	Line scanning direction. This bit controls line scanning direction. You must enable this bit for 90° or 270° rotation. For 90° rotation, set scanning to decrementing x-direction and incrementing y-direction and set the start address to the top-right corner of the image window and the start address must point to last pixel in 64-bit word. For 270° rotation, set scanning to incrementing x-direction and decrementing y-direction and set the start address to the bottom-left corner of the image window and the start address must point to first pixel in 64-bit word. For both 90° and 270° rotation, the absolute value of the stride must be programmed to integer multiple of 8-bytes plus 2 bytes. This stride programming may require additional padding bytes (up to two bytes per line) at the end of each line therefore may slightly increase the amount of memory requirement. Hardware cursor rotation must be done in software for 90° and 270° rotation.	0	Line scanning in X direction. This setting is used for 0° or 180° rotation.
		1	Line scanning in Y direction. This setting is used for 90° or 270° rotation.
14	Horizontal doubling. This bit controls pixel doubling in the horizontal direction and affects both the graphics image window and the cursor.	0	Pixels are not duplicated horizontally.
		1	Pixels are duplicated horizontally.
15	Vertical doubling. This bit controls vertical pixel doubling and affects both the graphics image window and the cursor.	0	Pixels are not duplicated vertically.
		1	Pixels are duplicated vertically.
17:16	GRCLK source. These bits select the clock source for the graphics controller root clock (GRCLK).	00	GRCLK source is the bus clock.
		01	GRCLK source is the first clock source.
		10	GRCLK source is the second clock source.
		11	GRCLK source is the third clock source.
18	Test mode. Set this bit to 0 for normal operation. This bit enables the factory color depth test mode when the main window buffer is enabled.	0	Disable test mode.
		1	Enable test mode.
19	Poly-Si TFT mode. Setting this bit enables support for poly-Si TFT mode that requires each line to be split into three lines: Blue-line, Green-line, and Red-line. This will cause each line to be read and processed three times	0	Disable Poly-Si TFT mode
		1	Enable Poly-Si TFT mode

Register 4-31: Graphics Controller Control Register (GC00R: Index 0h, Offset 180h)

Bit	Bit Definition	Bit Value	Value Definition
22:20	GMCLK first clock divisor (FD). These bits and bits [27:24] generate the controller master clock (GMCLK) from the root clock. These bits specify the divisor value for the first stage clock divider to generate GMCLK. The duty cycle for the output clock is not balanced except when FD = 1.	000	FD = 1
		001	FD = 1.5 Duty cycle is approximately 33 to 67.
		010	FD = 2.5 Duty cycle is approximately 40 to 60.
		011	FD = 3.5 Duty cycle is approximately 43 to 57.
		100	FD = 4.5 Duty cycle is approximately 44 to 56.
		101	FD = 5.5 Duty cycle is approximately 45 to 55.
		110	FD = 6.5 Duty cycle is approximately 46 to 54.
		111	Reserved.
23	Reserved. Must be programmed to 0.		
27:24	GMCLK Second Clock Divisor (SD). This parameter specifies the divisor value for the second stage clock divider which is used to divide the result of the first clock divisor to generate GMCLK. The divisor values ranges from 1 to 15. If this parameter is set to 0, GMCLK is disabled and GMCLK clock generation logic is powered down. GMCLK = GRCLK / FD / SD.		
30:28	Reserved Must be programmed to 0.		
31	Sharp 160x160 Hr-tft MODE This bit must be set for Sharp 160x160 HR-TFT panel to generate the vertical timing signals properly on FLCLK (CLS) and FLCLKA (PS). Note that FLCLKA must also be inverted.	0	Sharp 160x160 HR-TFT mode disabled.
		1	Sharp 160x160 HR-TFT mode enabled.

Register 4-32: Power Sequencing Control (GC01R: Index 04h, Offset 184h)

Bit	Bit Definition	Bit Value	Value Definition
2:0	Flat panel power-up interval. These bits specify the time from the activation of ENVDD to the activation of all flat-panel signals minus 1 frame time, or from the activation of ENCTL to the activation of ENVEE. For example: if the programmed value =2 frame time, this actual interval will be 3 frame times, etc.	000	1 frame time.
		001	2 frame time.
		010	4 frame time.
		011	8 frame time.
		100	16 frame time.
		101	32 frame time.
		110	48 frame time.
		111	64 frame time.
3	Fast power up. Set this bit to 0 during normal operation.	0	Power-up sequencing is active.
		1	Power-up sequencing is inactive. Enabling the graphics controller enables ENVDD, ENCTL, ENVEE, and the flat-panel data and control signals.

Register 4-32: Power Sequencing Control (GC01R: Index 04h, Offset 184h)

Bit	Bit Definition	Bit Value	Value Definition
6:4	Flat-panel power-down interval. Specifies the time from deactivating ENVEE to the deactivation of ENCTL, or from deactivation the flat-panel output signals to the deactivation of ENVDD minus 1 frame time. For example: if the programmed value = 2 frame times, then the actual interval between deactivation of the FP signals will be 3 frame times, etc.	000	1 frame time.
		001	2 frame time.
		010	4 frame time.
		011	8 frame time.
		100	16 frame time.
		101	32 frame time.
		110	48 frame time.
		111	64 frame time.
7	Fast power down. Set this bit to 0 during normal operation.	0	Power-down sequencing is active.
		1	Power-down sequencing is inactive. Enabling the graphics controller enables ENVDD, ENCTL, ENVEE, and the flat-panel data and control signals.
31:8	Reserved		

Register 4-33: Horizontal Display Control (GC02R: Index 08h, Offset 188h)

Bit	Bit Definition	Bit Value	Value Definition
10:0	Horizontal display total (HDT). Specifies the total length of the horizontal display and blank area in terms of number of pixels. Also marks the start of the next display line with respect to the start of the current line. Constraint: HDT ≥ HSE + 4 HSE is the horizontal synchronized end (see GC04R). Programmed value = actual value - 2		
15:11	Reserved		
26:16	Horizontal display end (HDE). Specifies the horizontal size of the display area in terms of the number of pixels. Programmed value = actual value		
31:27	Reserved		

Register 4-34: Vertical Display Control (GC03R: Index 0Ch, Offset 18Ch)

Bit	Bit Definition	Bit Value	Value Definition
9:0	Vertical display total (VDT). Specifies the total height of the vertical display and blank area in terms of number of lines. Also marks the start of the next frame with respect to the start of the current frame. Constraint: VDT ≥ VSI + 2 VSE is the vertical synchronized end (see GC05R). Programmed value = actual value - 1		
15:10	Reserved		
25:16	Vertical display end (VDE). Specifies the vertical size of the display area in terms of the number of lines. Programmed value = actual value -1		
31:26	Reserved		

Register 4-35: Horizontal Synchronization Control (GC04R: Index 10h, Offset 190h)

Bit	Bit Definition	Bit Value	Value Definition
10:0	Horizontal synch start (HSS). Specifies the horizontal synch start pulse start position in terms of number of pixels with respect to the left edge of the display area. Constraint: HSS ≥ HDE + 8 Programmed value = actual value		
15:11	Reserved		
26:16	Horizontal synch end (HSE). Specifies the horizontal synch pulse end position in terms of number of pixels with respect to the left edge of the display area. Constraint: HSE ≥ HSS + 4		
31:27	Reserved		

Register 4-36: Vertical Synchronization Control (GC05R: Index 14h, Offset 194h)

Bit	Bit Definition	Bit Value	Value Definition
9:0	Vertical synch start (VSS). Specifies the vertical synch start pulse start position in terms of number of lines with respect to the top edge of the display area. Constraint: VSS ≥ VDE + 1 Programmed value = actual value		
15:10	Reserved		
25:16	Vertical synch end (VSE). Specifies the vertical synch pulse end position in terms of number of lines with respect to the top edge of the display area. Constraint: VSE ≥ VSS + 1 Programmed value = vertical synch start + vertical synch height.		
31:26	Reserved		

Register 4-37: Horizontal Counter Initial Value (GC06R: Index 18h, Offset 198h)

Bit	Bit Definition	Bit Value	Value Definition
10:0	Horizontal counter initial value (HIV). Used to initialize the horizontal display counter for testing. Set to 000h for normal operation.		
11	Reserved		
15:12	Test mode bits. These bits are used for factory testing only and must be set to 0 during normal operation.		
31:16	Reserved		

Register 4-38: Vertical Counter Initial Value (GC07R: Index 1Ch, Offset 19Ch)

Bit	Bit Definition	Bit Value	Value Definition
9:0	Vertical counter initial value (VIV). Used to initialize the vertical display counter for testing. Set to 000h for normal operation.		
15:10	Reserved. Must be programmed to 0.		

Register 4-38: Vertical Counter Initial Value (GC07R: Index 1Ch, Offset 19Ch)

Bit	Bit Definition	Bit Value	Value Definition
31:16	Reserved		

Register 4-39: Horizontal Window Control (GC08R: Index 20Ch, Offset 1A0h)

Bit	Bit Definition	Bit Value	Value Definition
10:0	Horizontal window start (HWS). Specifies the graphics image window horizontal start position in terms of the number of lines with respect to the left edge of the display area. Programmed value = actual value		
15:11	Reserved		
26:16	Horizontal window width (HWW). Specifies the graphics image window height in terms of the number of lines. Constraint: HWW ≥ 8 Programmed value = actual value - 1 The horizontal window end (HWE) position with respect to the left edge of the display area is calculated from: HWS + HWW + 1		
31:27	Reserved		

Register 4-40: Vertical Window Control (GC09R: Index 24h, Offset 1A4h)

Bit	Bit Definition	Bit Value	Value Definition
0:9	Vertical window start (VWS). Specifies the graphics image window vertical start position in terms of the number of lines with respect to the top edge of the display area. Programmed value = actual value		
15:10	Reserved		
25:16	Vertical window height (VWH). Specifies the graphics image window height in terms of the number of lines. Constraint: VWH ≥ 1 Programmed value = actual value - 1 The vertical window end (VWE) position with respect to the left edge of the display area is calculated from: VWS + VWH + 1		
31:26	Reserved		

Register 4-41: Reserved (GC0AR: Index 28h, Offset 1A8h)

Bit	Bit Definition	Bit Value	Value Definition
31:0	Reserved		

The line clock which can be output on FLCLK is a pulse with the falling edge (start position) and rising edge (end position) within the horizontal timing region. Therefore, the frequency of this clock is the same as the line frequency. The pulse is always forced high at the beginning of the display line.

Register 4-42: Line Clock Control (GC0BR: Index 2Ch, Offset 1ACh)

Bit	Bit Definition	Bit Value	Value Definition
10:0	Line clock start (HLS). Specifies the horizontal line clock pulse start position in terms of the number of pixels with respect to the left edge of the display area. Programmed value = actual value		
15:11	Reserved		
26:16	Line clock end (HLE). Specifies the horizontal line clock pulse end position in terms of the number of pixels with respect to the left edge of the display area. Constraint: HLE ≥ HLS + 4 Programmed value = actual value		
31:27	Reserved		

Register 4-43: Window Start Address (GC0CR: Index 30h, Offset 1B0h)

Bit	Bit Definition	Bit Value	Value Definition
17:0	Window start address (WSA). Specifies the graphics image window start address in the display frame buffer for the main window buffer. This is a byte address; however, bit 0 must be 0 for 16 bpp. Additionally, bit 0 must be 0 for 8 bpp or less if scanning in incrementing x direction. Set bit 0 to 1 if scanning in the decrementing x direction.		
18	Reserved. Must be programmed to zero.		
31:19	Reserved		

Register 4-44: Alternate Window Start Address (GC0DR: Index 34h, Offset 1B4h)

Bit	Bit Definition	Bit Value	Value Definition
17:0	Alternate window start address (AWSA). Specifies the graphics image window start address in the display frame buffer for the alternate window buffer. This is a byte address; however, bit 0 must be 0 for 16 bpp. Additionally, bit 0 must be 0 for 8 bpp or less if scanning in incrementing x direction. Set bit 0 to 1 if scanning in the decrementing x direction.		
18	Reserved. Must be programmed to zero.		
31:19	Reserved		

Register 4-45: Window Stride (GC0ER: Index 38h, Offset 1B8h)

Bit	Bit Definition	Bit Value	Value Definition
15:0	Window Stride (WST). This parameter specifies the distance from the start of current line to the start of next line for the main window buffer. This is specified in terms of number of bytes and is programmed in 2's complement (signed) format. Negative stride (2's complement of absolute value of stride) must be programmed for 180° and 270° rotation. For 90° and 270° rotation, absolute value of the stride must be programmed to integer multiple of 8-bytes plus 2 bytes.		
31:16	Reserved		

Register 4-46: Reserved (GC0FR: Index 3Ch, Offset 1BCh)

Bit	Bit Definition	Bit Value	Value Definition
31:0	Reserved		

Both horizontal and vertical cursor starts should be changed with successive write cycles and the most significant bytes of this register must be written last. This register takes effect on the next falling edge of vertical synchronization following the write to the most significant bytes. The hardware cursor can be displayed anywhere within the display area.

Register 4-47: Hardware Cursor Position (GC10R: Index 40h, Offset 1C0h)

Bit	Bit Definition	Bit Value	Value Definition
10:0	Horizontal Cursor Start (HCS). Specifies the horizontal start position of the hardware cursor in terms of the number of pixels with respect to the left edge of the image window area. Programmed value = actual value		
15:11	Reserved		
25:16	Vertical cursor start (VCS). Specifies the vertical start position of the hardware cursor in terms of the number of lines with respect to the top edge of the image window area. Programmed value = actual value		
31:26	Reserved		

The hardware cursor start address and horizontal and vertical cursor offset should be changed with successive write cycles and the most significant bytes of this register must be written last. This register takes effect on the next falling edge of vertical synchronization following the write to the most significant bytes.

When an image window is scanned in decrementing x-direction, the hardware cursor is also scanned in decrementing x-direction. However, the hardware cursor's stride is always 16 bytes and the stride is always positive. Therefore, when scanning the image window in the decrementing y-direction, the hardware cursor must be vertically flipped by software. Also horizontal cursor offset calculation must be adjusted in software when scanning in the decrementing x-direction and vertical cursor offset calculation must be adjusted in software when scanning in the decrementing y-direction.

Register 4-48: Hardware Cursor Start Address and Offset (GC11R: Index 44h, Offset 1C4h)

Bit	Bit Definition	Bit Value	Value Definition
7:0	Hardware cursor start address (HCSA). This parameter specifies bits [17:10] of the start address of the hardware cursor in the display frame buffer. The start address is restricted to a 1024-byte boundary. Therefore, the lower 10 bits of this parameter are forced to 0.		
8	Reserved. Must be programmed to zero.		
15:9	Reserved		
21:16	Horizontal cursor offset (HCO). Specifies the horizontal offset of the hardware cursor in terms of the number of pixels with respect to the left edge of the cursor area. The hardware cursor horizontal offset specifies the first horizontal cursor pixel to be displayed. This parameter is used for left-edge clipping of the hardware cursor.		
23:22	Reserved		
29:24	Vertical cursor offset (VCO). Specifies the vertical offset of the hardware cursor in terms of the number of lines with respect to the top edge of the cursor area. The hardware cursor vertical offset specifies the first vertical cursor line displayed. This parameter is used for top-edge clipping of the hardware cursor.		
31:30	Reserved		

Register 4-49: Hardware Cursor Foreground Color (GC12R: Index 48h, Offset 1C8h)

Bit	Bit Definition	Bit Value	Value Definition
1:0	Reserved		
7:2	Hardware cursor foreground red color (HCFCR). Specifies the hardware cursor foreground red color.		
9:8	Reserved		
15:10	Hardware cursor foreground green color (HCFCG). Specifies the hardware cursor foreground green color. In monochrome mode, bits [15:14] are used as cursor foreground color bits [1:0].		
17:16	Reserved		
23:18	Hardware cursor foreground blue color (HCFCB). Specifies the hardware cursor foreground blue color. In monochrome mode, use bits [23:18] and [15:14] for the foreground color.		
31:24	Reserved		

Register 4-50: Hardware Cursor Background Color (GC13R: Index 4Ch, Offset 1CCh)

Bit	Bit Definition	Bit Value	Value Definition
1:0	Reserved		
7:2	Hardware cursor background red color (HCBCR). Specifies the hardware cursor background red color.		
9:8	Reserved		
15:10	Hardware cursor background green color (HCBCG). Specifies the hardware cursor background green color. In monochrome mode, bits [15:14] are used as cursor background color bits [1:0].		
17:16	Reserved		
23:18	Hardware cursor background blue color (HCBCB). Specifies the hardware cursor background blue color. In monochrome mode, use bits [23:18] and [15:14] for the background color.		
31:24	Reserved		

Register 4-51: Reserved (GC14R to GC19R: Index 50h, 54h, 58h, 5Ch, 60h, 64h, Offset 1D0h, 1D4h, 1D8h, 1DCh, 1E0h, 1E4h)

Bit	Bit Definition	Bit Value	Value Definition
31:0	Reserved		

The frame clock is a pulse with falling edge (start position) and rising edge (end position) within the vertical timing region, therefore the frequency of this clock is the same as the frame frequency. The pulse is always forced high at the beginning of the display line. This pulse can be output to flat panel and used as pulse-width modulation signal.

Register 4-52: Frame Clock Control (GC1AR: Index 68h, Offset 1E8h)

Bit	Bit Definition	Bit Value	Value Definition
9:0	Frame clock start (VFS). Specifies the vertical frame clock pulse start position in terms of the number of lines with respect to the top edge of the display area. Programmed value = actual value		
15:10	Reserved		
25:16	Frame clock end (VFE). Specifies the vertical frame clock pulse end position in terms of the number of lines with respect to the top edge of the display area. Constraint: VFE ≥ VFS + 1		
31:26	Reserved		

The GC1BR, GC1CR, GC1BR, and GC1CR registers read internal graphics controller signals for diagnostic and factory testing. They are read-only registers.

Register 4-53: Miscellaneous Signals - Read Only - (GC1BR: Index 6Ch, Offset 1ECh)

Bit	Bit Definition	Bit Value	Value Definition
0	GEHT Horizontal total greater than or equal to horizontal counter.		

Register 4-53: Miscellaneous Signals - Read Only - (GC1BR: Index 6Ch, Offset 1ECh)

Bit	Bit Definition	Bit Value	Value Definition
1	EQHS Horizontal synchronized start and end equal to horizontal counter.		
2	EQHW Horizontal window start and end equal to horizontal counter.		
3	EQHCS Horizontal cursor start equal to horizontal counter.		
4	EQHCE Horizontal cursor end equal to horizontal counter.		
5	EQHL Horizontal line clock start end equal to horizontal counter.		
6	Reserved.		
7	Reserved.		
8	GEVTA Vertical total greater than or equal to vertical counter.		
9	EQVSA Vertical synchronized start equal to vertical counter.		
10	EQVWA Vertical window start and end equal to vertical counter.		
11	EQVCA Vertical cursor start and end equal to vertical counter.		
12	EQVFA Vertical frame clock start and end equal to vertical counter.		
13	Reserved.		
31:14	Reserved.		

Register 4-54: Horizontal Parameter - Read Only - (GC1CR: Index 70h, Offset 1F0h)

Bit	Bit Definition	Bit Value	Value Definition
10:0	Horizontal display counter (GHCNT). Internal horizontal display counter. This is a fast counter; therefore, the read value may not be reliable in normal operation.		
11	Reserved.		
22:12	Horizontal window end (HWE).		
23	Reserved.		
29:24	Horizontal cursor end (HCE). Internal horizontal cursor end position.		
31:30	Reserved.		

Register 4-55: Vertical Parameter - Read Only - (GC1DR: Index 74h, Offset 1F4h)

Bit	Bit Definition	Bit Value	Value Definition
9:0	Vertical display counter (GVCNT). Internal vertical display counter. This is a relatively slow counter, but its value may change when read in normal operation.		
11:10	Reserved.		
21:12	Vertical window end (VWE). Internal vertical window end position.		
23:22	Reserved.		
29:24	Vertical cursor end (VCE). Internal vertical cursor end position.		
31:30	Reserved.		

Register 4-56: Window Line Start Address - Read Only - (GC1ER: Index 78h, Offset 1F8h)

Bit	Bit Definition	Bit Value	Value Definition
18:0	Window line start address (GWSA). Internal window line start address bits [18:0]. This value may change when read in normal operation.		
19	Reserved.		
28:20	Window byte count bits [11:3] (GWBC). Internal line byte count bits [11:3]. This value may change when read in normal operation.		
31:29	Reserved.		

The GC1FR register reads internal graphics controller signals for diagnostic and factory testing. Do not write to this register during normal operation because its internal write enable pulse is used for test mode. This is a read-only register.

Register 4-57: Cursor Line Start Address - Read Only - (GC1FR: Index 7Ch, Offset, Offset 1FCh)

Bit	Bit Definition	Bit Value	Value Definition
3:0	Reserved.		
18:4	Cursor line start address (GCSA). Internal cursor line start address bits [18:4]. This value may change when read in normal operation.		
31:19	Reserved.		

4.9.3. Graphics Controller Color Palette

The color palette is implemented as a single 256 x 18-bit color palette. Registers CP00 through CPFF have indexes of 000h through 3FC, increasing by increments of four, and the reset value x-xxxxh.

Register 4-58: Graphics Controller Color Palette (CP00 - CPFF: Index 000 - 3FC, Offset 800 - BFC)

Bit	Bit Definition	Bit Value	Value Definition
1:0	Reserved		
7:2	Red color palette. Specifies red color values.		
9:8	Reserved		
15:10	Green color palette. Specifies green color values. In monochrome mode, bits [15:14] are used as monochrome palette bits [7:6].		
17:16	Reserved		

Register 4-58: Graphics Controller Color Palette (CP00 - CPFF: Index 000 - 3FC, Offset 800 - BFC)

Bit	Bit Definition	Bit Value	Value Definition
23:18	Blue color palette. Specifies blue color values. In monochrome mode, bits [23:18] and [15:14] are used as monochrome palette output bits [5:0] and [7:6], respectively.		
31:24	Reserved		

4.10 Flat-Panel Interface

The flat-panel interface (FPI) converts the output of the graphics controller into data that will be provided directly to the flat panel display. The MQ-1100/1132 FPI module supports a direct interface to both mono/color S-STN panels and mono/color TFT panels. Furthermore, additional control signals have been provided in order to directly interface to low cost TFT panels that do not implement a traditional timing controller on board. These include gate and source driver inputs as well as a line clock.

A proprietary dithering algorithm is implemented to improve display quality on TFT panels. In addition, a programmable proprietary grayscaling (frame rate control [FRC]) and dithering algorithm are implemented to provide high-quality display on STN panels. Sufficient programmability is built-in to allow fine-tuning of the gray scaling quality for STN panels. The FRC provides 16-level gray scaling without dithering and up to 64-level grays with dithering. The MQ-1100/1132 supports the following panels:

- 4-bit, 8-bit, and 16-bit monochrome S-STN panel
- 4-bit, 8-bit, and 16-bit color S-STN panel
- 4-bit, 6-bit, and 8-bit monochrome TFT panel
- 9-bit, 12-bit and 18-bit color TFT panel
- Direct support for 18-Bit Sharp HR-TFT
- Direct support for 18-bit POLY-Si TFT

For TFT panels, only 1-pixel-per-clock panels are supported.

The maximum pixel clock frequency for the FPI is 48 MHz for both TFT and STN panels.

Flat panel power sequencing is provided as part of the graphics controller logic.

Two programmable pulse-width-modulation signals are provided on PWM0 and PWM1 pins. The source of these signals is either the fast oscillator clock or CPU Interface clock or internal HSYNC signal.

4.10.1. Flat-Panel Register Definition

Table 4-10 specifies the index, offset and reset values for the Flat-Panel registers.

TABLE 4-10: Flat-Panel Register Index and Reset Values

Register	Index	Offset	Reset Value	See Description
FP00R	00h	600h	0000-0000h	*Register 4-59 on page 109*
FP01R	04h	604h	0000-0000h	*Register 4-60 on page 110*
FP02R	08h	608h	0FFC-FCFFh	*Register 4-61 on page 112*
FP03R	0Ch	60Ch	0000-0000h	*Register 4-62 on page 114*
FP04R	10h	610h	0000-0000h	*Register 4-63 on page 116*
FP05R	14h	614h	0000-0000h	*Register 4-64 on page 117*
FP06R	18h	618h	0000-0000h	*Register 4-65 on page 119*
FP07R	1Ch	61Ch	0000-0000h	*Register 4-66 on page 121*
FP08R	20h	620h	xxxx-xxxxh	*Register 4-67 on page 121*
FP09R	24h	624h	xxxx-xxxxh	*Register 4-68 on page 121*
FP0AR	28h	628h	F003-0000h	*Register 4-69 on page 122*
FP0BR	2Ch	62Ch	xxxx-x000h	*Register 4-70 on page 124*
FP0ER	38h	638h	xxxx-xx00h	*Register 4-71 on page 125*
FP0FR	3Ch	63Ch	0000-0000h	*Register 4-72 on page 125*
FP10R to FP2FR	40h to BCh	640-6BCh	xxxx-xxxxh	*Register 4-73 on page 127*
FP30R to FP37R	C0h to DCh	6C0-6DCh	xxxx-xxxxh	*Register 4-74 on page 127*
FP30R	C0h	6C0h	xxxx-xxxxh	*Register 4-75 on page 128*
FP31R	C4h	6C4h	xxxx-xxxxh	*Register 4-76 on page 129*
FP32R	C8h	6C8h	xxxx-xxxxh	*Register 4-77 on page 129*
FP33R	CCh	6CCh	xxxx-xxxxh	*Register 4-78 on page 129*
FP34R	D0h	6D0h	xxxx-xxxxh	*Register 4-79 on page 129*
FP35R	D4h	6D4h	xxxx-xxxxh	*Register 4-80 on page 130*
FP36R	D8h	6D8h	xxxx-xxxxh	*Register 4-81 on page 130*
FP37R	DCh	6DCh	xxxx-xxxxh	*Register 4-82 on page 130*

Register 4-59 through *Register 4-82 on page 130* specify the Flat Panel control register bit values and definitions.

Register 4-59: Flat Panel Control Register (FP00R: Index 00h, Offset 600h)

Bit	Bit Definition	Bit Value	Value Definition
1:0	Reserved Must be programmed to 0		
3:2	Flat Panel Type These bits indicate type of flat panel.	00	TFT panel.
		01	S-STN panel (single-panel single-drive)
		1x	Reserved
4	Monochrome or Color Panel Select This bit selects mono/color panel.	0	Color panel
		1	Monochrome panel.
7:5	Flat Panel Interface This parameter specifies the panel data width.	000	TFT: 4-bit monochrome or 12-bit color interface S-STN: 4-bit monochrome or 4-bit color interface
		001	TFT: 6-bit monochrome or 18-bit color interface S-STN: 8-bit monochrome or 8-bit color interface
		010	TFT: 8-bit mono
		011	S-STN: 16-bit monochrome or 16-bit color interface
		(others reserved)	Reserved
9:8	Dither Pattern These bits select dither pattern.	00	Reserved
		01	Dither pattern 1
		10	Reserved
		11	Reserved
11:10	Reserved These bits must be programmed to 0.		
14:12	Dither Base Color These bits select the number of bits to be dithered.	000	Dither is disabled.
		001	Reserved.
		010	Reserved.
		011	3 bits. This setting should be used with 3-bits per color TFT or 8-level FRC for STN panels.
		100	4 bits. This setting should be used with 4-bit/color TFT or 16-level FRC for STN panels.
		101	5 bits -- This setting should be used with monochrome panel only
		110	6 bits -- This setting should be used with monochrome panel only
		111	Reserved
15	Alternate Window Control Setting this bit disable dither and FRC in Alternate Window mode.	0	Dither and FRC can be enabled when Alternate Window is enabled.
		1	Disable dither and FRC when Alternate Window is enabled.
17:16	FRC Control These bits control grayscaling for STN panels. These bits have no effect on TFT panels.	00	2-level FRC -- This setting essentially disable the FRC. The FRC logic will take the most significant bits of input color data as FRC output data.
		01	4-level FRC
		10	8-level FRC
		11	16-level FRC
18	Reserved This bit must be programmed to 0.		
19	Poly-Si TFT mode Setting this bit enables support for poly-Si TFT mode that divides shift clock by 3 and select a single color to output to the panel for each line. This bit also causes FMOD signal to toggle every 3 lines.	0	Disable Poly-Si TFT mode
		1	Enable Poly-Si TFT mode

Register 4-59: Flat Panel Control Register (FP00R: Index 00h, Offset 600h)

Bit	Bit Definition	Bit Value	Value Definition
20	Poly-Si TFT First Line This bit is effective only when FP00R[19] is set to 1.	0	First Red, Green, Blue lines data are not forced to all ones.
		1	First Red, Green, Blue lines data are forced to all ones.
21	Poly-Si TFT display data control This bit is effective only when FPOOR[19] is set to 1. Setting this bit will make bit 20 ineffective.	0	All display lines data are not forced to all ones.
		1	All display lines data are forced to all ones.
27:22	Reserved These bits must be programmed to 0.		
28	Test Mode 0 Setting this bit enables factory test mode for FPI module. This bit must be programmed to 0 in normal operation.	0	Disable test mode for FPI.
		1	Enable test mode for FPI.
29	Test Mode 1 Setting this bit enables factory test mode for FPI module. This bit must be programmed to 0 in normal operation.	0	Disable test mode for FPI.
		1	Enable test mode for FPI.
30	Test Mode 2 Setting this bit enables factory test mode for FPI module. This bit must be programmed to 0 in normal operation.	0	Disable Test mode for FPI.
		1	Enable test mode for FPI.
31	Test Mode 3 Setting this bit enables factory test mode for FPI module. This bit must be programmed to 0 in normal operation.	0	Disable test mode for FPI.
		1	Enable test mode for FPI.

Register 4-60: Flat-Panel Pin Control (FP01R: Index 04h, Offset 604h)

Bit	Bit Definition	Bit Value	Value Definition
0	Disable Flat Panel pins Setting this bit disable all flat panel data and control (FD[23:18], FD[15:10], FD[7:2], FSCLK, FDE, FHSYNC, FVSYNC, FMOD, FLCLK) pins.	0	Enable the flat panel data and control signals pins.
		1	Flat panel data and control signals pins are driven low.
1	Reserved This bit must be programmed to 0.		
2	Flat panel Display Enable Control This bit controls generation of FDE signal.	0	FDE pin outputs flat panel composite display enable signal.
		1	FDE pin outputs flat panel horizontal display enable signal.
3	Flat panel AC Modulation Enable This bit enables FMOD signal generation. FMOD signal is normally used only on some STN panels but this bit is effective regardless of panel type (TFT/STN).	0	Disable FMOD signal generation.
		1	Enable FMOD signal generation. FP04R[31:24] controls the generation of FMOD signal.
4	Reserved This bit must be programmed to 0.		
5	Flat panel PWM Clock Enable This bit enables FPWMCLK signal generation.	0	Disable FPWMCLK signal generation.
		1	Enable FPWMCLK signal generation.

Register 4-60: Flat-Panel Pin Control (FP01R: Index 04h, Offset 604h)

Bit	Bit Definition	Bit Value	Value Definition
6	TFT Shift Clock Select This bit is effective for TFT panel only. Setting this bit will essentially divide shift clock by 2 for panels that require data on both falling and rising edges.	0	Output data can be latched externally on falling edge of shift clock (FSCLK).
		1	Output data can be latched externally on both rising and falling edges of shift clock (FSCLK).
7	Shift Clock Mask This bit controls shift clock output (FSCLK) during non-display area.	0	Allow shift clock to run during non-display area.
		1	Force shift clock low during non-display area.
8	FHSYNC (LP) Control This bit controls FHSYNC (LP) output during vertical blank area.	0	Enable the FHSYNC (LP) during vertical blank time. For STN panel, bit 9 is effective for this setting but bit 10 is ignored.
		1	Disable the FHSYNC (LP) during vertical blank time. For STN panel, bit 9 is ignored but bit 10 is effective for this setting. Also for STN panel, shift clock (FSCLK) will also be disabled during vertical blank time
9	STN Shift Clock Control (STN panel only) This bit is effective for STN panel only when bit 8 is reset to 0. This bit controls shift clock output during vertical blank area.	0	Enable the shift clock for all lines in the vertical blank area.
		1	Disable the Shift clock for all lines in the vertical blank area.
10	STN Extra LP Enable (STN panel only) This bit is effective for STN panel only when bit 8 is set to 1. When this bit is enabled, extra LP is generated at the end of first line of vertical blank time.	0	Disable the extra LP
		1	Enable the extra LP
11	Reserved This bit must be programmed to 0.		
13:12	TFT Display Enable Select This parameter selects the signal that goes out on FDE pin for TFT panels. For STN panels, display enable is normally not used and if needed then this parameter should be programmed to 00.	00	FDE pin outputs either horizontal or composite display enable signal (as selected by bit 2).
		01	FDE pin outputs source driver start pulse which is a one clock pulse generated one clock before the first data of each active line.
		10	FDE pin outputs early horizontal or composite display enable signal (as selected by bit 2) which is one clock earlier than data.
		11	FDE pin outputs extended horizontal or composite display enable signal (as selected by bit 2) which is activated one clock earlier than first pixel data but deactivated at same time with last pixel data.
15:14	TFT Horizontal Sync Select This parameter selects the signal that goes out on FHSYNC pin for TFT panels. For STN panel, this parameter should be programmed to 00.	00	FHSYNC pin outputs horizontal sync signal.
		01	FHSYNC pin outputs a line pulse signal which is a one clock cycle pulse generated three clocks after horizontal sync trailing edge.
		10	FHSYNC pin outputs a line pulse signal which is a two clock cycle pulse generated three clocks after horizontal sync trailing edge.
		11	FHSYNC pin outputs a line pulse signal which is a three clock cycle pulse generated three clocks after horizontal sync trailing edge.
17:16	TFT Vertical Sync Select This parameter selects the signal that goes out on FVSYNC pin for TFT panels. For STN panel, FLM goes out on FVSYNC pin so this parameter is not used.	00	FVSYNC pin outputs the first line marker (FLM) in the first line of the display.
		01	FVSYNC pin outputs early vertical sync signal which is two clocks prior to leading edge of horizontal sync.
		10	FVSYNC pin outputs late vertical sync signal which is two clocks after the leading edge of horizontal sync.
		11	FVSYNC pin outputs vertical sync signal on trailing edge of horizontal sync.

Register 4-60: Flat-Panel Pin Control (FP01R: Index 04h, Offset 604h)

Bit	Bit Definition	Bit Value	Value Definition
18	Line Clock Control This bit controls the behavior of flat panel line clock (FLCLK) during vertical blank.	0	FLCLK is enabled during the first line of vertical blank and disabled for the rest of vertical blank. If FLCLK is active high then it will be driven low during vertical blank time and if FLCLK is active low then it will be driven high during vertical blank time.
		1	FLCLK is enabled during vertical blank.
19	Alternate Line Clock Control This bit controls the behavior of flat panel line clock during vertical blank when it is output on PWM1 pin.	0	Alternate line clock is enabled during the first line of vertical blank and disabled for the rest of vertical blank. If it is active high then it will be driven low during vertical blank time and if it is active low then it will be driven high during vertical blank time.
		1	Alternate line clock is enabled during vertical blank.
20	FMOD Clock Control This bit controls the active edge of the clock that generate FMOD.	0	FMOD is generated with negative edge of its clock.
		1	FMOD is generated with positive edge of its clock.
21	FMOD Frame Inversion This bit controls frame inversion of FMOD. This bit should be set only when FMOD is generated using line clock.	0	FMOD inversion is not forced every frame however inversion may still depend on FMODE cycles and vertical total parameter.
		1	FMOD Inversion is inverted every frame.
22	FMOD Frequency Control This bit controls inversion of FMOD. This bit should be set only when FMOD is generated using line clock.	0	FMOD frequency is determined by the count value programmed in FP04R[30:24].
		1	FMOD changes when ENB signal is low (see FP06R[30] bit description).
23	FMOD Synchronous Reset Setting this bit enables synchronous reset of FMOD at the beginning of the frame. This bit should be set only when FMOD is generated using line clock. If vertical total is even number of lines, setting this bit causes FMOD to be inverted every frame.	0	FMOD polarity is not reset at the beginning of frame.
		1	FMOD polarity is reset at the beginning of frame.
26:24	Flat Panel Shift Clock (FSCLK) Delay This parameter provides programmable delay on FSCLK output pin ranging from 0 to 7 ns typically.		
27	Flat panel Extended Line Clock Control This bit controls the behavior of flat panel line clock (FLCLK) and alternate line clock (FLCLKA) during the first line of vertical blank when either bit 18 or bit 19 is set to 0.	0	FLCLK/FLCLKA is disabled during the first line of vertical blank.
		1	FLCLK/FLCLKA is enabled during the first line of vertical blank.
31:28	Reserved These bits must be programmed to 0.		

Register 4-61: Flat-Panel Pin Control (FP02R: Index 08h, Offset 608h)

Bit	Bit Definition	Bit Value	Value Definition
0	Flat Panel ENVDD Output Control This bit controls the flat panel ENVDD pin output buffer.	0	Disable the flat panel ENVDD output.
		1	Enable the flat panel ENVDD output.
1	Flat Panel ENVEE Output Control This bit controls the flat panel ENVEE pin output buffer.	0	Disable the flat panel ENVEE output.
		1	Enable the flat panel ENVEE output.
2	Flat Panel Data Bit Output Control This bit controls the flat panel FD2 pin output buffer.	0	Disable the flat panel FD2 output.
		1	Enable the flat panel FD2 output.

Register 4-61: Flat-Panel Pin Control (FP02R: Index 08h, Offset 608h)

Bit	Bit Definition	Bit Value	Value Definition
3	Flat Panel Data Bit Output Control This bit controls the flat panel FD3 pin output buffer.	0	Disable the flat panel FD3 output.
		1	Enable the flat panel FD3 output.
4	Flat Panel Data Bit Output Control This bit controls the flat panel FD4 pin output buffer.	0	Disable the flat panel FD4 output.
		1	Enable the flat panel FD4 output.
5	Flat Panel Data Bit Output Control This bit controls the flat panel FD5 pin output buffer.	0	Disable the flat panel FD5 output.
		1	Enable the flat panel FD5 output.
6	Flat Panel Data Bit Output Control This bit controls the flat panel FD6 pin output buffer.	0	Disable the flat panel FD6 output.
		1	Enable the flat panel FD6 output.
7	Flat Panel Data Bit Output Control This bit controls the flat panel FD7 pin output buffer.	0	Disable the flat panel FD7 output.
		1	Enable the flat panel FD7 output.
9-8	Reserved These bits must be programmed to 0.		
10	Flat Panel Data Bit Output Control This bit controls the flat panel FD10 pin output buffer.	0	Disable the flat panel FD10 output.
		1	Enable the flat panel FD10 output.
11	Flat Panel Data Bit Output Control This bit controls the flat panel FD11 pin output buffer.	0	Disable the flat panel FD11 output.
		1	Enable the flat panel FD11 output.
12	Flat Panel Data Bit Output Control This bit controls the flat panel FD12 pin output buffer.	0	Disable the flat panel FD12 output.
		1	Enable the flat panel FD12 output.
13	Flat Panel Data Bit Output Control This bit controls the flat panel FD13 pin output buffer.	0	Disable the flat panel FD13 output.
		1	Enable the flat panel FD13 output.
14	Flat Panel Data Bit Output Control This bit controls the flat panel FD14 pin output buffer.	0	Disable the flat panel FD14 output.
		1	Enable the flat panel FD14 output.
15	Flat Panel Data Bit Output Control This bit controls the flat panel FD15 pin output buffer.	0	Disable the flat panel FD15 output.
		1	Enable the flat panel FD15 output.
17:16	Reserved These bits must be programmed to 0.		
18	Flat Panel Data Bit Output Control This bit controls the flat panel FD18 pin output buffer.	0	Disable the flat panel FD18 output.
		1	Enable the flat panel FD18 output.
19	Flat Panel Data Bit Output Control This bit controls the flat panel FD19 pin output buffer.	0	Disable the flat panel FD19 output.
		1	Enable the flat panel FD19 output.
20	Flat Panel Data Bit Output Control This bit controls the flat panel FD20 pin output buffer.	0	Disable the flat panel FD20 output.
		1	Enable the flat panel FD20 output.
21	Flat Panel Data Bit Output Control This bit controls the flat panel FD21 pin output buffer.	0	Disable the flat panel FD21 output.
		1	Enable the flat panel FD21 output.

Register 4-61: Flat-Panel Pin Control (FP02R: Index 08h, Offset 608h)

Bit	Bit Definition	Bit Value	Value Definition
22	Flat Panel Data Bit Output Control This bit controls the flat panel FD22 pin output buffer.	0	Disable the flat panel FD22 output.
		1	Enable the flat panel FD22 output.
23	Flat Panel Data Bit Output Control This bit controls the flat panel FD23 pin output buffer.	0	Disable the flat panel FD23 output.
		1	Enable the flat panel FD23 output.
24	Flat Panel Shift Clock (FSCLK) Output Control This bit controls the FSCLK pin output buffer.	0	Disable the FSCLK output.
		1	Enable the FSCLK output.
25	Flat Panel Data Enable (FDE) Output Control This bit controls the FDE pin output buffer.	0	Disable the FDE output.
		1	Enable the FDE output.
26	Flat Panel Horizontal Sync (FHSYNC) Output Control This bit controls the FHSYNC pin output buffer.	0	Disable the FHSYNC output.
		1	Enable the FHSYNC output.
27	Flat Panel Vertical Sync (FVSYNC) Output Control This bit controls the FVSYNC pin output buffer.	0	Disable the FVSYNC output.
		1	Enable the FVSYNC output.
28	Flat Panel Modulation Clock (FMOD) Output Control This bit controls the FMOD pin output buffer.	0	Disable the FMOD output.
		1	Enable the FMOD output.
29	Flat Panel Line Clock (FLCLK) Output Control This bit controls the FLCLK pin output buffer.	0	Disable the FLCLK output.
		1	Enable the FLCLK output.
30	Pulse Width Modulation 0 (PWM0) Output Control This bit controls the PWM0 pin output buffer.	0	Disable the PWM0 output.
		1	Enable the PWM0 output.
31	Pulse Width Modulation 1 (PWM1) Output Control This bit controls the PWM1 pin output buffer.	0	Disable the PWM1 output.
		1	Enable the PWM1 output.

Register 4-62: Flat Panel Pin Input Control (FP03R: Index 0Ch, Offset 60Ch)

Bit	Bit Definition	Bit Value	Value Definition
0	Flat Panel ENVDD Input Control This bit controls the flat panel ENVDD pin input buffer.	0	Disable the flat panel ENVDD input.
		1	Enable the flat panel ENVDD input. Input data can be read from FP09R[0].
1	Flat Panel ENVEE Input Control This bit controls the flat panel ENVEE pin input buffer.	0	Disable the flat panel ENVEE input.
		1	Enable the flat panel ENVEE input. Input data can be read from FP09R[1].
2	Flat Panel Data Bit Input Control This bit controls the flat panel FD2 pin input buffer.	0	Disable the flat panel FD2 input.
		1	Enable the flat panel FD2 input. Input data can be read from FP09R[2].

Register 4-62: Flat Panel Pin Input Control (FP03R: Index 0Ch, Offset 60Ch)

Bit	Bit Definition	Bit Value	Value Definition
3	Flat Panel Data Bit Input Control This bit controls the flat panel FD3 pin input buffer.	0	Disable the flat panel FD3 input.
		1	Enable the flat panel FD3 input. Input data can be read from FP09R[3].
4	Flat Panel Data Bit Input Control This bit controls the flat panel FD4 pin input buffer.	0	Disable the flat panel FD4 input.
		1	Enable the flat panel FD4 input. Input data can be read from FP09R[4].
5	Flat Panel Data Bit Input Control This bit controls the flat panel FD5 pin input buffer.	0	Disable the flat panel FD5 input.
		1	Enable the flat panel FD5 input. Input data can be read from FP09R[5].
6	Flat Panel Data Bit Input Control This bit controls the flat panel FD6 pin input buffer.	0	Disable the flat panel FD6 input.
		1	Enable the flat panel FD6 input. Input data can be read from FP09R[6].
7	Flat Panel Data Bit Input Control This bit controls the flat panel FD7 pin input buffer.	0	Disable the flat panel FD7 input.
		1	Enable the flat panel FD7 input. Input data can be read from FP09R[7].
9:8	Reserved These bits must be programmed to 0.		
10	Flat Panel Data Bit Input Control This bit controls the flat panel FD10 pin input buffer.	0	Disable the flat panel FD10 input.
		1	Enable the flat panel FD10 input. Input data can be read from FP09R[10].
11	Flat Panel Data Bit Input Control This bit controls the flat panel FD11 pin input buffer.	0	Disable the flat panel FD11 input.
		1	Enable the flat panel FD11 input. Input data can be read from FP09R[11].
12	Flat Panel Data Bit Input Control This bit controls the flat panel FD12 pin input buffer.	0	Disable the flat panel FD12 input.
		1	Enable the flat panel FD12 input. Input data can be read from FP09R[12].
13	Flat Panel Data Bit Input Control This bit controls the flat panel FD13 pin input buffer.	0	Disable the flat panel FD13 input.
		1	Enable the flat panel FD13 input. Input data can be read from FP09R[13].
14	Flat Panel Data Bit Input Control This bit controls the flat panel FD14 pin input buffer.	0	Disable the flat panel FD14 input.
		1	Enable the flat panel FD14 input. Input data can be read from FP09R[14].
15	Flat Panel Data Bit Input Control This bit controls the flat panel FD15 pin input buffer.	0	Disable the flat panel FD15 input.
		1	Enable the flat panel FD15 input. Input data can be read from FP09R[15].
17:16	Reserved These bits must be programmed to 0.		
18	Flat Panel Data Bit Input Control This bit controls the flat panel FD18 pin input buffer.	0	Disable the flat panel FD18 input.
		1	Enable the flat panel FD18 input. Input data can be read from FP09R[18].
19	Flat Panel Data Bit Input Control This bit controls the flat panel FD19 pin input buffer.	0	Disable the flat panel FD19 input.
		1	Enable the flat panel FD19 input. Input data can be read from FP09R[19].
20	Flat Panel Data Bit Input Control This bit controls the flat panel FD20 pin input buffer.	0	Disable the flat panel FD20 input.
		1	Enable the flat panel FD20 input. Input data can be read from FP09R[20].
21	Flat Panel Data Bit Input Control This bit controls the flat panel FD21 pin input buffer.	0	Disable the flat panel FD21 input.
		1	Enable the flat panel FD21 input. Input data can be read from FP09R[21].

Register 4-62: Flat Panel Pin Input Control (FP03R: Index 0Ch, Offset 60Ch)

Bit	Bit Definition	Bit Value	Value Definition
22	Flat Panel Data Bit Input Control This bit controls the flat panel FD22 pin input buffer.	0	Disable the flat panel FD22 input.
		1	Enable the flat panel FD22 input. Input data can be read from FP09R[22].
23	Flat Panel Data Bit Input Control This bit controls the flat panel FD23 pin input buffer.	0	Disable the flat panel FD23 input.
		1	Enable the flat panel FD23 input. Input data can be read from FP09R[23].
24	Flat Panel Shift Clock (FSCLK) Input Control This bit controls the FSCLK pin input buffer.	0	Disable the FSCLK input.
		1	Enable the FSCLK input. Input data can be read from FP09R[24].
25	Flat Panel Data Enable (FDE) Input Control This bit controls the FDE pin input buffer.	0	Disable the FDE input.
		1	Enable the FDE input. Input data can be read from FP09R[25].
26	Flat Panel Horizontal Sync (FHSYNC) Input Control This bit controls the FHSYNC pin input buffer.	0	Disable the FHSYNC input.
		1	Enable the FHSYNC input. Input data can be read from FP09R[26].
27	Flat Panel Vertical Sync (FVSYNC) Input Control This bit controls the FVSYNC pin input buffer.	0	Disable the FVSYNC input.
		1	Enable the FVSYNC input. Input data can be read from FP09R[27].
28	Flat Panel Modulation Clock (FMOD) Input Control This bit controls the FMOD pin input buffer.	0	Disable the FMOD input.
		1	Enable the FMOD input. Input data can be read from FP09R[28].
29	Flat Panel Line Clock (FLCLK) Input Control This bit controls the FLCLK pin input buffer.	0	Disable the FLCLK input.
		1	Enable the FLCLK input. Input data can be read from FP09R[29].
30	Pulse Width Modulation 0 (PWM0) Input Control This bit controls the PWM0 pin input buffer.	0	Disable the PWM0 input.
		1	Enable the PWM0 input. Input data can be read from FP09R[30].
31	Pulse Width Modulation 1 (PWM1) Input Control This bit controls the PWM1 pin input buffer.	0	Disable the PWM1 input.
		1	Enable the PWM1 input. Input data can be read from FP09R[31].

Register 4-63: STN Panel Control (FP04R: Index 10h, Offset 610h)

Bit	Bit Definition	Bit Value	Value Definition
7:0	FRC tuning control bits. Specifies tuning value for FRC algorithm.		
15:8	FRC tuning control bits. Specifies tuning value for FRC algorithm.		
23:16	FRC tuning control bits. Specifies tuning value for FRC algorithm.		
30:24	Flat-panel modulation period. This parameter specifies half of the period of the FMOD signal for STN and TFT panels. FMOD signal is generated either using internal vertical sync or internal horizontal sync, depending on the setting of bit 31. This bit is effective only if FP01R[22] is 0. Programmed value = (actual period / 2) – 1.		

Register 4-63: STN Panel Control (FP04R: Index 10h, Offset 610h)

Bit	Bit Definition	Bit Value	Value Definition
31	Flat-panel modulation clock select. Controls the clock used to generate the FMOD signal. The FMOD signal changes four clocks after the leading edge of the internal-horizontal synchronization.	0	Internal vertical sync generates FMOD.
		1	Internal horizontal sync generates FMOD.

Register 4-64: Flat-Panel Pin Polarity Control (FP05R: Index 14h, Offset 614h)

Bit	Bit Definition	Bit Value	Value Definition
1:0	Reserved These bits must be programmed to 0.		
2	Flat Panel Data Bit Polarity This bit controls the polarity of the flat panel FD2 output pin.	0	Flat panel FD2 output is active high.
		1	Flat panel FD2 output is active low.
3	Flat Panel Data Bit Polarity This bit controls the polarity of the flat panel FD3 output pin.	0	Flat panel FD3 output is active high.
		1	Flat panel FD3 output is active low.
4	Flat Panel Data Bit Polarity This bit controls the polarity of the flat panel FD4 output pin.	0	Flat panel FD4 output is active high.
		1	Flat panel FD4 output is active low.
5	Flat Panel Data Bit Polarity This bit controls the polarity of the flat panel FD5 output pin.	0	Flat panel FD5 output is active high.
		1	Flat panel FD5 output is active low.
6	Flat Panel Data Bit Polarity This bit controls the polarity of the flat panel FD6 output pin.	0	Flat panel FD6 output is active high.
		1	Flat panel FD6 output is active low.
7	Flat Panel Data Bit Polarity This bit controls the polarity of the flat panel FD7 output pin.	0	Flat panel FD7 output is active high.
		1	Flat panel FD7 output is active low.
9:8	Reserved These bits must be programmed to 0.		
10	Flat Panel Data Bit Polarity This bit controls the polarity of the flat panel FD10 output pin.	0	Flat panel FD10 output is active high.
		1	Flat panel FD10 output is active low.
11	Flat Panel Data Bit Polarity This bit controls the polarity of the flat panel FD11 output pin.	0	Flat panel FD11 output is active high.
		1	Flat panel FD11 output is active low.
12	Flat Panel Data Bit Polarity This bit controls the polarity of the flat panel FD12 output pin.	0	Flat panel FD12 output is active high.
		1	Flat panel FD12 output is active low.
13	Flat Panel Data Bit Polarity This bit controls the polarity of the flat panel FD13 output pin.	0	Flat panel FD13 output is active high.
		1	Flat panel FD13 output is active low.
14	Flat Panel Data Bit Polarity This bit controls the polarity of the flat panel FD14 output pin.	0	Flat panel FD14 output is active high.
		1	Flat panel FD14 output is active low.
15	Flat Panel Data Bit Polarity This bit controls the polarity of the flat panel FD15 output pin.	0	Flat panel FD15 output is active high.
		1	Flat panel FD15 output is active low.
17:16	Reserved These bits must be programmed to 0.		

Register 4-64: Flat-Panel Pin Polarity Control (FP05R: Index 14h, Offset 614h)

Bit	Bit Definition	Bit Value	Value Definition
18	Flat Panel Data Bit Polarity This bit controls the polarity of the flat panel FD18 output pin.	0	Flat panel FD18 output is active high.
		1	Flat panel FD18 output is active low.
19	Flat Panel Data Bit Polarity This bit controls the polarity of the flat panel FD19 output pin.	0	Flat panel FD19 output is active high.
		1	Flat panel FD19 output is active low.
20	Flat Panel Data Bit Polarity This bit controls the polarity of the flat panel FD20 output pin.	0	Flat panel FD20 output is active high.
		1	Flat panel FD20 output is active low.
21	Flat Panel Data Bit Polarity This bit controls the polarity of the flat panel FD21 output pin.	0	Flat panel FD21 output is active high.
		1	Flat panel FD21 output is active low.
22	Flat Panel Data Bit Polarity This bit controls the polarity of the flat panel FD22 output pin.	0	Flat panel FD22 output is active high.
		1	Flat panel FD22 output is active low.
23	Flat Panel Data Bit Polarity This bit controls the polarity of the flat panel FD23 output pin.	0	Flat panel FD23 output is active high.
		1	Flat panel FD23 output is active low.
24	Flat Panel Shift Clock (FSCLK) Polarity This bit controls the polarity of the FSCLK output pin.	0	FSCLK output is active high. Data is output on rising edge of FSCLK and should be latched externally with falling edge of FSCLK.
		1	FSCLK output is active low. Data is output on falling edge of FSCLK and should be latched externally with rising edge of FSCLK.
25	Flat Panel Data Enable (FDE) Polarity This bit controls the polarity of the FDE pin.	0	FDE output is active high.
		1	FDE output is active low.
26	Flat Panel Horizontal Sync (FHSYNC) Polarity This bit controls the polarity of the FHSYNC pin.	0	FHSYNC output is active high.
		1	FHSYNC output is active low.
27	Flat Panel Vertical Sync (FVSYNC) Polarity This bit controls the polarity of the FVSYNC pin.	0	FVSYNC output is active high.
		1	FVSYNC output is active low.
28	Flat Panel Modulation Clock (FMOD) Polarity This bit controls the polarity of the FMOD pin.	0	FMOD output is active high.
		1	FMOD output is active low.
29	Flat Panel Line Clock (FLCLK) Polarity This bit controls the polarity of the FLCLK pin.	0	FLCLK output is active high.
		1	FLCLK output is active low.
30	Pulse Width Modulation 0 (PWM0) Polarity This bit controls the polarity of the PWM0 pin.	0	PWM0 output is active high.
		1	PWM0 output is active low.
31	Pulse Width Modulation 1 (PWM1) Polarity This bit controls the polarity of the PWM1 pin.	0	PWM1 output is active high.
		1	PWM1 output is active low.

Register 4-65: Flat-Panel Pin Output Select 0 (FP06R: Index 18h, Offset 618h)

Bit	Bit Definition	Bit Value	Value Definition
0	Flat Panel ENVDD Output Select 0 This bit and FD07R[0] control output of flat panel ENVDD pin.	0	If FP07R[0]=0, the flat panel ENVDD pin outputs Enable VDD signal. If FP07R[0]=1, flat panel ENVDD pin outputs FP08R[0].
		1	If FP07R[0]=0, flat panel ENVDD pin outputs Enable CTL signal. If FP07R[0]=1, flat panel ENVDD pin is used for testing.
1	Flat Panel ENVEE Output Select 0 This bit and FD07R[1] control output of flat panel ENVEE pin.	0	If FP07R[1]=0, flat panel ENVEE pin outputs Enable VEE signal. If FP07R[1]=1, flat panel ENVEE pin outputs FP08R[1].
		1	If FP07R[1]=0, flat panel ENVEE pin outputs Enable CTL signal. If FP07R[1]=1, flat panel ENVEE pin is used for testing.
2	Flat Panel Data bit 2 Output Select 0 This bit and FD07R[2] control output of flat panel FD2 pin.	0	If FP07R[2]=0, flat panel FD2 pin outputs TFT data bit 2. If FP07R[2]=1, flat panel FD2 pin outputs FP08R[2].
		1	If FP07R[2]=0, flat panel FD2 pin outputs STN data bit 2. If FP07R[2]=1, flat panel FD2 pin is used for testing.
3	Flat Panel Data bit 3 Output Select 0 This bit and FD07R[3] control output of flat panel FD3 pin.	0	If FP07R[3]=0, flat panel FD3 pin outputs TFT data bit 3. If FP07R[3]=1, flat panel FD3 pin outputs FP08R[3].
		1	If FP07R[3]=0, flat panel FD3 pin outputs STN data bit 3. If FP07R[3]=1, flat panel FD3 pin is used for testing.
4	Flat Panel Data bit 4 Output Select 0 This bit and FD07R[4] control output of flat panel FD4 pin.	0	If FP07R[4]=0, flat panel FD4 pin outputs TFT data bit 4. If FP07R[4]=1, flat panel FD4 pin outputs FP08R[4].
		1	If FP07R[4]=0, flat panel FD4 pin outputs STN data bit 4. If FP07R[4]=1, flat panel FD4 pin is used for testing.
5	Flat Panel Data bit 5 Output Select 0 This bit and FD07R[5] control output of flat panel FD5 pin.	0	If FP07R[5]=0, flat panel FD5 pin outputs TFT data bit 5. If FP07R[5]=1, flat panel FD5 pin outputs FP08R[5].
		1	If FP07R[5]=0, flat panel FD5 pin outputs STN data bit 5. If FP07R[5]=1, flat panel FD5 pin is used for testing.
6	Flat Panel Data bit 6 Output Select 0 This bit and FD07R[6] control output of flat panel FD6 pin.	0	If FP07R[6]=0, flat panel FD6 pin outputs TFT data bit 6. If FP07R[6]=1, flat panel FD6 pin outputs FP08R[6].
		1	If FP07R[6]=0, flat panel FD6 pin outputs STN data bit 6. If FP07R[6]=1, flat panel FD6 pin is used for testing.
7	Flat Panel Data bit 7 Output Select 0 This bit and FD07R[7] control output of flat panel FD7 pin.	0	If FP07R[7]=0, flat panel FD7 pin outputs TFT data bit 7. If FP07R[7]=1, flat panel FD7 pin outputs FP08R[7].
		1	If FP07R[7]=0, flat panel FD7 pin outputs STN data bit 7. If FP07R[7]=1, flat panel FD7 pin is used for testing.
9:8	Reserved These bits must be programmed to 0.		
10	Flat Panel Data bit 10 Output Select 0 This bit and FD07R[10] control output of flat panel FD10 pin.	0	If FP07R[10]=0, flat panel FD10 pin outputs TFT data bit 10. If FP07R[10]=1, flat panel FD10 pin outputs FP08R[10].
		1	If FP07R[10]=0, flat panel FD10 pin outputs STN data bit 10. If FP07R[10]=1, flat panel FD10 pin is used for testing.
11	Flat Panel Data bit 11 Output Select 0 This bit and FD07R[11] control output of flat panel FD11 pin.	0	If FP07R[11]=0, flat panel FD11 pin outputs TFT data bit 11. If FP07R[11]=1, flat panel FD11 pin outputs FP08R[11].
		1	If FP07R[11]=0, flat panel FD11 pin outputs STN data bit 11. If FP07R[11]=1, flat panel FD11 pin is used for testing.
12	Flat Panel Data bit 12 Output Select 0 This bit and FD07R[12] control output of flat panel FD12 pin.	0	If FP07R[12]=0, flat panel FD12 pin outputs TFT data bit 12. If FP07R[12]=1, flat panel FD12 pin outputs FP08R[12].
		1	If FP07R[12]=0, flat panel FD12 pin outputs STN data bit 12. If FP07R[12]=1, flat panel FD12 pin is used for testing.

Register 4-65: Flat-Panel Pin Output Select 0 (FP06R: Index 18h, Offset 618h)

Bit	Bit Definition	Bit Value	Value Definition
13	Flat Panel Data bit 13 Output Select 0 This bit and FD07R[13] control output of flat panel FD13 pin.	0	If FP07R[13]=0, flat panel FD13 pin outputs TFT data bit 13. If FP07R[13]=1, flat panel FD13 pin outputs FP08R[13].
		1	If FP07R[13]=0, flat panel FD13 pin outputs STN data bit 13. If FP07R[13]=1, flat panel FD13 pin is used for testing.
14	Flat Panel Data bit 14 Output Select 0 This bit and FD07R[14] control output of flat panel FD14 pin.	0	If FP07R[14]=0, flat panel FD14 pin outputs TFT data bit 14. If FP07R[14]=1, flat panel FD14 pin outputs FP08R[14].
		1	If FP07R[14]=0, flat panel FD14 pin outputs STN data bit 14. If FP07R[14]=1, flat panel FD14 pin is used for testing.
15	Flat Panel Data bit 15 Output Select 0 This bit and FD07R[15] control output of flat panel FD15 pin.	0	If FP07R[15]=0, flat panel FD15 pin outputs TFT data bit 15. If FP07R[15]=1, flat panel FD15 pin outputs FP08R[15].
		1	If FP07R[15]=0, flat panel FD15 pin outputs STN data bit 15. If FP07R[15]=1, flat panel FD15 pin is used for testing.
17:16	Reserved These bits must be programmed to 0.		
18	Flat Panel Data bit 18 Output Select 0 This bit and FD07R[18] control output of flat panel FD18 pin.	0	If FP07R[18]=0, flat panel FD18 pin outputs TFT data bit 18. If FP07R[18]=1, flat panel FD18 pin outputs FP08R[18].
		1	If FP07R[18]=0, flat panel FD18 pin outputs STN data bit 18. If FP07R[18]=1, flat panel FD18 pin is used for testing.
19	Flat Panel Data bit 19 Output Select 0 This bit and FD07R[19] control output of flat panel FD19 pin.	0	If FP07R[19]=0, flat panel FD19 pin outputs TFT data bit 19. If FP07R[19]=1, flat panel FD19 pin outputs FP08R[19].
		1	If FP07R[19]=0, flat panel FD19 pin outputs STN data bit 19. If FP07R[19]=1, flat panel FD19 pin is used for testing.
20	Flat Panel Data bit 20 Output Select 0 This bit and FD07R[20] control output of flat panel FD20 pin.	0	If FP07R[20]=0, flat panel FD20 pin outputs TFT data bit 20. If FP07R[20]=1, flat panel FD20 pin outputs FP08R[20].
		1	If FP07R[20]=0, flat panel FD20 pin outputs STN data bit 20. If FP07R[20]=1, flat panel FD20 pin is used for testing.
21	Flat Panel Data bit 21 Output Select 0 This bit and FD07R[21] control output of flat panel FD21 pin.	0	If FP07R[21]=0, flat panel FD21 pin outputs TFT data bit 21. If FP07R[21]=1, flat panel FD21 pin outputs FP08R[21].
		1	If FP07R[21]=0, flat panel FD21 pin outputs STN data bit 21. If FP07R[21]=1, flat panel FD21 pin is used for testing.
22	Flat Panel Data bit 22 Output Select 0 This bit and FD07R[22] control output of flat panel FD22 pin.	0	If FP07R[22]=0, flat panel FD22 pin outputs TFT data bit 22. If FP07R[22]=1, flat panel FD22 pin outputs FP08R[22].
		1	If FP07R[22]=0, flat panel FD22 pin outputs STN data bit 22. If FP07R[22]=1, flat panel FD22 pin is used for testing.
23	Flat Panel Data bit 23 Output Select 0 This bit and FD07R[23] control output of flat panel FD23 pin.	0	If FP07R[23]=0, flat panel FD23 pin outputs TFT data bit 23. If FP07R[23]=1, flat panel FD23 pin outputs FP08R[23].
		1	If FP07R[23]=0, flat panel FD23 pin outputs STN data bit 23. If FP07R[23]=1, flat panel FD23 pin is used for testing.
24	Flat Panel Shift Clock (FSCLK) Output Select 0 This bit and FD07R[24] control output of FSCLK pin.	0	If FP07R[24]=0, flat panel FSCLK pin outputs TFT shift clock. If FP07R[24]=1, flat panel FSCLK pin outputs FP08R[24].
		1	If FP07R[24]=0, flat panel FSCLK pin outputs STN shift clock. If FP07R[24]=1, flat panel FSCLK pin is used for testing.
25	Flat Panel Data Enable (FDE) Output Select 0 This bit and FD07R[25] control output of FDE pin.	0	If FP07R[25]=0, flat panel FDE pin outputs TFT data enable or source driver start pulse. If FP07R[25]=1, flat panel FDE pin outputs FP08R[25].
		1	If FP07R[25]=0, flat panel FDE pin outputs STN data enable. If FP07R[25]=1, flat panel FDE pin outputs FPWMCLK signal.

Register 4-65: Flat-Panel Pin Output Select 0 (FP06R: Index 18h, Offset 618h)

Bit	Bit Definition	Bit Value	Value Definition
26	Flat Panel Horizontal Sync (FHSYNC) Output Select 0 This bit and FD07R[26] control output of FHSYNC pin.	0	If FP07R[26]=0, flat panel FHSYNC pin outputs TFT horizontal sync or line pulse, depending on the setting of the FPO1R[15:4] If FP07R[26]=1, flat panel FHSYNC pin outputs FP08R[26].
		1	If FP07R[26]=0, flat panel FHSYNC pin outputs STN line pulse. If FP07R[26]=1, flat panel FHSYNC pin is used for testing.
27	Flat Panel Vertical Sync (FVSYNC) Output Select 0 This bit and FD07R[27] control output of FVSYNC pin.	0	If FP07R[27]=0, flat panel FVSYNC pin outputs TFT vertical sync or gate driver start pulse, depending on the setting of the FPO1R[17:16] If FP07R[27]=1, flat panel FVSYNC pin outputs FP08R[27].
		1	If FP07R[27]=0, flat panel FVSYNC pin outputs STN first line marker. If FP07R[27]=1, flat panel FVSYNC pin is used for testing.
28	Flat Panel Modulation Clock (FMOD) Output Select 0 This bit and FD07R[28] control output of FMOD pin.	0	If FP07R[28]=0, flat panel FMOD pin outputs TFT/STN modulation clock. If FP07R[28]=1, flat panel FMOD pin outputs FP08R[28].
		1	If FP07R[28]=0, flat panel FMOD pin is used for testing. If FP07R[28]=1, flat panel FMOD pin is used for testing.
29	Flat Panel Line Clock (FLCLK) Output Select 0 This bit and FD07R[29] control output of FLCLK pin.	0	If FP07R[29]=0, flat panel FLCLK pin outputs flat panel line clock. If FP07R[29]=1, flat panel FLCLK pin outputs FP08R[29].
		1	If FP07R[29]=0, flat panel FLCLK pin outputs FPWMCLK signal. If FP07R[29]=1, flat panel FLCLK pin is used for testing.
30	Pulse Width Modulation 0 (PWM0) Output Select 0 This bit and FD07R[30] control output of PWM0 pin.	0	If FP07R[30]=0, flat panel PWM0 pin outputs PWM0 signal. If FP07R[30]=1, flat panel PWM0 pin outputs FP08R[30].
		1	If FP07R[30]=0, flat panel PWM0 pin outputs Frame Clock signal (see GC1AR register). If FP07R[30]=1, flat panel PWM0 pin outputs active low horizontal blank time (ENB) between Blue-line and Green-line (once every three lines) for Poly-Si TFT panel.
31	Pulse Width Modulation 1 (PWM1) Output Select 0 This bit and FD07R[31] control output of PWM1 pin.	0	If FP07R[31]=0, flat panel PWM1 pin outputs PWM1. If FP07R[31]=1, flat panel PWM1 pin outputs FP08R[31].
		1	If FP07R[31]=0, flat panel PWM1 pin outputs FLCLK. If FP07R[31]=1, flat panel PWM1 pin outputs modulation clock which is unaffected by FP01R[21].

Register 4-66: Flat-Panel Pin Output Select 1 (FP07R: Index 1Ch, Offset 61Ch)

Bit	Bit Definition	Bit Value	Value Definition
31:0	Flat-panel pin output select 1. These bits and the corresponding bits in FP06R control the output signals on FPI pins.		

Register 4-67: Flat-Panel Pin Output Data (FP08R: Index 20h, Offset 620h)

Bit	Bit Definition	Bit Value	Value Definition
31:0	Flat-panel pin output data. These bits can be output on FPI pins when they are selected as output pins (see FP06R).		

Register 4-68: Flat-Panel Pin Input Data (Read Only) (FP09R: Index 24h, Offset 624h)

Bit	Bit Definition	Bit Value	Value Definition
31:0	Flat-panel pin input data. The FPI pins can be read on these bits when the corresponding pin input buffer is enabled (see FP03R).		

Register 4-69: Flat-Panel Pin Weak Pull-Down Control (FP0AR: Index 28h, Offset 628h)

Bit	Bit Definition	Bit Value	Value Definition
0	Flat Panel ENVDD Weak Pull-Down Control This bit controls weak pull-down of flat panel ENVDD pin.	0	Disable the flat panel ENVDD weak pull-down.
		1	Enable the flat panel ENVDD weak pull-down.
1	Flat Panel ENVEE Weak Pull-Down Control This bit controls weak pull-down of flat panel ENVEE pin.	0	Disable the flat panel ENVEE weak pull-down.
		1	Enable the flat panel ENVEE weak pull-down.
2	Flat Panel Data Bit Weak Pull-Down Control This bit controls the flat panel FD2 pin weak pull-down.	0	Disable the flat panel FD2 weak pull-down.
		1	Enable the flat panel FD2 weak pull-down.
3	Flat Panel Data Bit Weak Pull-Down Control This bit controls the flat panel FD3 pin weak pull-down.	0	Disable the flat panel FD3 weak pull-down.
		1	Enable the flat panel FD3 weak pull-down.
4	Flat Panel Data Bit Weak Pull-Down Control This bit controls the flat panel FD4 pin weak pull-down.	0	Disable the flat panel FD4 weak pull-down.
		1	Enable the flat panel FD4 weak pull-down.
5	Flat Panel Data Bit Weak Pull-Down Control This bit controls the flat panel FD5 pin weak pull-down.	0	Disable the flat panel FD5 weak pull-down.
		1	Enable the flat panel FD5 weak pull-down.
6	Flat Panel Data Bit Weak Pull-Down Control This bit controls the flat panel FD6 pin weak pull-down.	0	Disable the flat panel FD6 weak pull-down.
		1	Enable the flat panel FD6 weak pull-down.
7	Flat Panel Data Bit Weak Pull-Down Control This bit controls the flat panel FD7 pin weak pull-down.	0	Disable the flat panel FD7 weak pull-down.
		1	Enable the flat panel FD7 weak pull-down.
9:8	Reserved These bits must be programmed to 0.		
10	Flat Panel Data Bit Weak Pull-Down Control This bit controls the flat panel FD10 pin weak pull-down.	0	Disable the flat panel FD10 weak pull-down.
		1	Enable the flat panel FD10 weak pull-down.
11	Flat Panel Data Bit Weak Pull-Down Control This bit controls the flat panel FD11 pin weak pull-down.	0	Disable the flat panel FD11 weak pull-down.
		1	Enable the flat panel FD11 weak pull-down.
12	Flat Panel Data Bit Weak Pull-Down Control This bit controls the flat panel FD12 pin weak pull-down.	0	Disable the flat panel FD12 weak pull-down.
		1	Enable the flat panel FD12 weak pull-down.
13	Flat Panel Data Bit Weak Pull-Down Control This bit controls the flat panel FD13 pin weak pull-down.	0	Disable the flat panel FD13 weak pull-down.
		1	Enable the flat panel FD13 weak pull-down.
14	Flat Panel Data Bit Weak Pull-Down Control This bit controls the flat panel FD14 pin weak pull-down.	0	Disable the flat panel FD14 weak pull-down.
		1	Enable the flat panel FD14 weak pull-down.
15	Flat Panel Data Bit Weak Pull-Down Control This bit controls the flat panel FD15 pin weak pull-down.	0	Disable the flat panel FD15 weak pull-down.
		1	Enable the flat panel FD15 weak pull-down.
17:16	Reserved		
18	Flat Panel Data Bit Weak Pull-Down Control This bit controls the flat panel FD18 pin weak pull-down.	0	Disable the flat panel FD18 weak pull-down.
		1	Enable the flat panel FD18 weak pull-down.

Register 4-69: Flat-Panel Pin Weak Pull-Down Control (FP0AR: Index 28h, Offset 628h)

Bit	Bit Definition	Bit Value	Value Definition
19	Flat Panel Data Bit Weak Pull-Down Control This bit controls the flat panel FD19 pin weak pull-down.	0	Disable the flat panel FD19 weak pull-down.
		1	Enable the flat panel FD19 weak pull-down.
20	Flat Panel Data Bit Weak Pull-Down Control This bit controls the flat panel FD20 pin weak pull-down.	0	Disable the flat panel FD20 weak pull-down.
		1	Enable the flat panel FD20 weak pull-down.
21	Flat Panel Data Bit Weak Pull-Down Control This bit controls the flat panel FD21 pin weak pull-down.	0	Disable the flat panel FD21 weak pull-down.
		1	Enable the flat panel FD21 weak pull-down.
22	Flat Panel Data Bit Weak Pull-Down Control This bit controls the flat panel FD22 pin weak pull-down.	0	Disable the flat panel FD22 weak pull-down.
		1	Enable the flat panel FD22 weak pull-down.
23	Flat Panel Data Bit Weak Pull-Down Control This bit controls the flat panel FD23 pin weak pull-down.	0	Disable the flat panel FD23 weak pull-down.
		1	Enable the flat panel FD23 weak pull-down.
24	Flat Panel Shift Clock (FSCLK) Weak Pull-Down Control This bit controls the FSCLK pin weak pull-down.	0	Disable the FSCLK weak pull-down.
		1	Enable the FSCLK weak pull-down.
25	Flat Panel Data Enable (FDE) Weak Pull-Down Control This bit controls the FDE pin weak pull-down.	0	Disable the FDE weak pull-down.
		1	Enable the FDE weak pull-down.
26	Flat Panel Horizontal Sync (FHSYNC) Weak Pull-Down Control This bit controls the FHSYNC pin weak pull-down.	0	Disable the FHSYNC weak pull-down.
		1	Enable the FHSYNC weak pull-down.
27	Flat Panel Vertical Sync (FVSYNC) Weak Pull-Down Control This bit controls the FVSYNC pin weak pull-down.	0	Disable the FVSYNC weak pull-down.
		1	Enable the FVSYNC weak pull-down.
31:28	Reserved		

Register 4-70: Flat Panel Additional Pin Output Select (FP0BR: Index: 2Ch, Offset 62Ch)

Bit	Bit Definition	Bit Value	Value Definition
1:0	**Flat Panel ENVDD Output Select 3-2** This bit controls ENVDD output when FP07R[0]=0 and FP06R[0]=1.	00	Flat Panel ENVDD pin outputs Enable CTL signal.
		01	Flat Panel ENVDD pin outputs Enable VEE signal.
		10	Flat Panel ENVDD pin outputs PWM0 signal.
		11	Flat Panel ENVDD pin outputs Codec Serial Master Clock (SMCLK) signal.
3:2	**Flat Panel ENVEE Output Select 3-2** This bit controls ENVEE output when FP07R[1]=0 and FP06R[1]=1.	00	Flat Panel ENVEE pin outputs Enable CTL signal.
		01	Flat Panel ENVEE pin outputs T3D[0].
		10	Flat Panel ENVEE pin outputs PWM1 signal.
		11	Flat Panel ENVEE pin outputs Codec Serial Data Out (SOUT) signal.
5:4	**Flat Panel FMOD Output Select 3-2** This bit controls FMOD output when FP07R[28]=0 and FP06R[28]=1. In input mode, this pin can be used as Codec Serial Root Clock (SRCLK) input.	00	Flat Panel FMOD pin outputs LED.
		01	Flat Panel FMOD pin outputs Enable VDD signal.
		10	Flat Panel FMOD pin outputs Enable VEE signal.
		11	Flat Panel FMOD pin outputs PWM0 signal.
7:6	**Flat Panel FLCLK Output Select 3-2** This bit controls FLCLK output when FP07R[29]=0 and FP06R[29]=1. In input mode, this pin can be used as Codec Serial Bit Clock (SCLK) input.	00	Flat Panel FLCLK pin outputs FPWMCLK signal.
		01	Flat Panel FLCLK pin outputs LED.
		10	Flat Panel FLCLK pin outputs PWM0 signal.
		11	Flat Panel FLCLK pin outputs Codec Serial Bit Clock (SCLK) signal.
9:8	**Flat Panel PWM0 Output Select 3-2** This bit controls PWM0 output when FP07R[30]=0 and FP06R[30]=1. In input mode, this pin can be used as Codec Frame Synchronization (FSYNC) input.	00	Flat Panel PWM0 pin outputs FMOD.
		01	Flat Panel PWM0 pin outputs T3D[8].
		10	Flat Panel PWM0 pin outputs T3D[9].
		11	Flat Panel PWM0 pin outputs Codec Frame Synchronization (FSYNC) signal.
11:10	**Flat Panel PWM1 Output Select 3-2** This bit controls PWM1 output when FP07R[31]=0 and FP06R[31]=1. In input mode, this pin can be used as Codec Serial Data Input (SIN).	00	Flat Panel PWM1 pin outputs alternate FLCLK.
		01	Flat Panel PWM1 pin outputs internal FHSYNC which is running during vertical blank time.
		10	Flat Panel PWM1 pin outputs Vertical Display Enable.
		11	Flat Panel PWM1 pin outputs LED.
31:12	Reserved		

Register 4-71: Flat-Panel Test Control (FP0ER: Index 38h, Offset 638h)

Bit	Bit Definition	Bit Value	Value Definition
0	CRC Enable This bit enables the CRC logic and is only effective when the TFT panel is programmed.	0	Disable the CRC.
		1	Enable the CRC.
2:1	CRC Input Data Control This parameter selects input data for CRC logic.	00	Wait for 1 VSYNC before capturing data for CRC logic. Captures one frame of data.
		01	Wait for 2 VSYNC before capturing data for CRC logic. Captures one frame of data.
		10	Continuous capturing of CRC data.
		11	Reserved.
3	Reserved This bit must be programmed to 0.		
5:4	Test Output Select This parameter selects the test output data read in bits [31:8]. The CRC result can be read on bits [29:8] while bit 0 is still set. CRC result is reset to zeros when bit 0 is reset. (factory test mode only)	00	Read 22-bit CRC result for blue datapath.
		01	Read 22-bit CRC result for green datapath.
		10	Read 22-bit CRC result for red datapath.
		11	Read 24-bit FRC test point. The CRC can be disabled when reading the FRC test point.
7:6	Reserved These bits must be programmed to 0.		
31:8	Test Result Data (Read Only) These bits returns test result data as selected by bits [5:4]. (factory test mode only)		

Register 4-72: Pulse Width Modulation Control (FP0FR: Index 3Ch, Offset 63Ch)

Bit	Bit Definition	Bit Value	Value Definition
1:0	PWM 0 Source Clock These bits control the source of PWM 0 clock.	00	PWM 0 signal is generated using oscillator clock.
		01	PWM 0 signal is generated using bus clock.
		10	PWM 0 signal is generated using internal horizontal sync signal.
		11	Reserved.
2	PWM 0 Sequencing This bit controls PWM 0 sequencing when PWM 0 is enabled.	0	PWM 0 sequencing is tied to flat panel power sequencing. PWM 0 signal will be generated when flat panel data/control signals are enabled, and it will be deactivated when flat panel data/control signals are disabled.
		1	PWM 0 generation is not tied to flat panel power sequencing. PWM 0 signal will always be generated when it is enabled except when the source clock is internal horizontal sync signal.
3	Reserved This bit must be programmed to 0.		
7:4	PWM 0 Clock Pre-Divider This parameter specifies the divisor value for the PWM 0 clock. The divisor value ranges from 1 to 15. If this parameter is set to 0, PWM 0 source clock is disabled and therefore PWM 0 generation logic is powered down.		

Register 4-72: Pulse Width Modulation Control (FP0FR: Index 3Ch, Offset 63Ch)

Bit	Bit Definition	Bit Value	Value Definition
15:8	PWM 0 Duty Cycle This parameter specifies the number of clock high time for PWM 0 pulse. Note that the period of PWM 0 signal is always 256 clocks. If this parameter is programmed to 0 then the PWM 0 will generate one clock pulse every 256-clock cycle and if this parameter is programmed to FFh then the PWM 0 will be static high signal. If enabled, the PWM 0 signal starts before the ENCTL pin is activated (high) and ends after the ENCTL pin is deactivated (low). When PWM 0 is inactive, the PWM 0 signal is also driven low.		
17:16	PWM 1 Source Clock These bits control the source of PWM 1 clock.	00	PWM 1 signal is generated using oscillator clock.
		01	PWM 1 signal is generated using bus clock.
		10	PWM 1 signal is generated using internal horizontal sync signal.
		11	Reserved
18	PWM 1 Sequencing This bit controls PWM 1 sequencing when PWM 1 is enabled.	0	PWM 1 sequencing is tied to flat panel power sequencing. PWM 1 signal is activated when the flat panel data and control signals are enabled and is deactivated when the flat panel data and control signals are disabled.
		1	PWM 1 generation is not tied to flat panel power sequencing. PWM 1 signal will always be generated when it is enabled except when the source clock is internal horizontal sync signal.
19	Reserved		
23:20	PWM 1 Clock Pre-Divider This parameter specifies the divisor value for the PWM 1 clock. The divisor value ranges from 1 to 15. If this parameter is set to 0, PWM 1 source clock is disabled and therefore PWM 1 generation logic is powered down.		
31:24	PWM 1 Duty Cycle This parameter specifies the number of clock high time for PWM 1 pulse. The PWM 1 signal's period is always 256 clocks. If this parameter is programmed to 0 then PWM 1 generates one clock pulse every 256 clock cycles. If this parameter is programmed to FFh, then PWM 1 is a static high signal. If enabled, the PWM 1 signal starts before the ENCTL pin is activated (high) and ends after the ENCTL pin is deactivated (low). During period where PWM 1 is inactive, the PWM 1 signal is also driven low.		

Register 4-73: FRC Pattern (FP10R to FP2FR - FRC Pattern: Index, 40h to BCH, Offset 640-6BCh)

Bit	Bit Definition	Bit Value	Value Definition
31:0	These registers specify FRC patterns. FRC utility is provided to change this pattern.		

The function of registers FP30R-FP37R is controlled by the setting of FP01R bit 5. If this bit is set to 0, the description found in *Register 4-74* applies and these eight registers set the FRC weight values. If this bit is set to 1, apply the descriptions of *Register 4-75* through *Register 4-82*.

Register 4-74: FRC Weight (FP30R to FP37R - FRC Weight: Index, C0h to DCH, Offset 6C0-6DCh)

Bit	Bit Definition	Bit Value	Value Definition
31:0	These registers specify FRC weights. FRC utility is provided to change this data.		

Note: *Depending on the CPU interface used, the mapping of the FRC pattern (FP10R-FP2FR) and the FRC Weight (FP30-FP37R) is different. For the Motorola Dragonball and PCI interfaces, the mapping is as described above. For the SA-11xx, NEC 41xx and Hitachi 77xx processors, the registers need to be accessed differently as follows:*

FRC Pattern Register

-FP10R-FP1FR (index 40h-7Fh)	Read / Writes perform normally
-FP20R-FP2FR (Index 80h-BFh)	Mapped to FP30R-FP3FR (Index C0h-FFh)

FRC Weight Register

-FP30R-FP37R (index C0h-DCh)	Mapped to FP70R-FP77R Index 1C0h-1DCh)

The following FRC weight registers (*Register 4-75* through *Register 4-82*) are also used to generate the FPWMCLK signal for PWM flat panels.These can be reflected on either the FDE or the FLCLK pin, depending on the configuration of the register bits FP01R[5], FP06R[25] and FP06R[29].The PWM clock for PWM panels is generated starting at the trailing edge of the FHSYNC (LP) pulse when FP01R[5] is set to 1. The PWM clock runs continuously until the next leading edge of FHSYNC (LP) pulse.

Register 4-75: Flat-Panel PWM Clock Control (FP30R: Index C0h, Offset 6C0h)

Bit	Bit Definition	Bit Value	Value Definition
4:0	Flat panel PWM Clock Cycle Time This parameters specifies the cycle time of the flat panel PWM clock.	0000x	1.0 clock cycles: 0.5 clock high time, 0.5 clock low time.
		00010	2.0 clock cycles: 1.0 clock high time, 1.0 clock low time.
		00011	1.5 clock cycles: 1.0 clock high time, 0.5 clock low time.
		00100	3.0 clock cycles: 1.5 clock high time, 1.5 clock low time.
		00101	2.5 clock cycles: 1.0 clock high time, 1.5 clock low time.
		00110	4.0 clock cycles: 2.0 clock high time, 2.0 clock low time.
		00111	3.5 clock cycles: 2.0 clock high time, 1.5 clock low time.
		01000	5.0 clock cycles: 2.5 clock high time, 2.5 clock low time.
		01001	4.5 clock cycles: 2.0 clock high time, 2.5 clock low time.
		01010	6.0 clock cycles: 3.0 clock high time, 3.0 clock low time.
		01011	5.5 clock cycles: 3.0 clock high time, 2.5 clock low time.
		01100	7.0 clock cycles: 3.5 clock high time, 3.5 clock low time.
		01101	6.5 clock cycles: 3.0 clock high time, 3.5 clock low time.
		01110	8.0 clock cycles: 4.0 clock high time, 4.0 clock low time.
		01111	7.5 clock cycles: 4.0 clock high time, 3.5 clock low time.
		10000	9.0 clock cycles: 4.5 clock high time, 4.5 clock low time.
		10001	8.5 clock cycles: 4.0 clock high time, 4.5 clock low time.
		10010	10.0 clock cycles: 5.0 clock high time, 5.0 clock low time.
		10011	9.5 clock cycles: 5.0 clock high time, 4.5 clock low time.
		10100	11.0 clock cycles: 5.5 clock high time, 5.5 clock low time.
		10101	10.5 clock cycles: 5.0 clock high time, 4.5 clock low time.
		10110	12.0 clock cycles: 6.0 clock high time, 6.0 clock low time.
		10111	11.5 clock cycles: 6.0 clock high time, 5.5 clock low time.
		11000	13.0 clock cycles: 6.5 clock high time, 6.5 clock low time.
		11001	12.5 clock cycles: 6.0 clock high time, 6.5 clock low time.
		11010	14.0 clock cycles: 7.0 clock high time, 7.0 clock low time.
		11011	13.5 clock cycles: 7.0 clock high time, 6.5 clock low time.
		11100	15.0 clock cycles: 7.5 clock high time, 7.5 clock low time.
		11101	14.5 clock cycles: 7.0 clock high time, 7.5 clock low time.
		11110	16.0 clock cycles: 8.0 clock high time, 8.0 clock low time.
		11111	15.5 clock cycles: 8.0 clock high time, 7.5 clock low time.
7:5	Reserved		
10:8	Flat panel PWM Clock Delay This parameters specifies the initial clock delay of the first rising edge of FPWMCLK with respect to falling edge of FHSYNC (LP) measured in pixel clock. Programmed value = actual value + 1. Actual value can range from -1 to 4 pixel clocks.	000	First rising edge of PWM clock is one clock earlier than falling edge of LP.
		001	First rising edge of PWM clock is at the same time as falling edge of LP ime.
		010	First rising edge of PWM clock is one clock later than falling edge of LP.
		011	First rising edge of PWM clock is two clocks later than falling edge of LP
		100	First rising edge of PWM clock is three clocks later than falling edge of LP.
		101	First rising edge of PWM clock is four clocks later than falling edge of LP.
		110	Reserved.
		111	Reserved.
31:11	Reserved		

Register 4-76: FRC Weight (FP31R: Index 0C4h, Offset 6C4h)

Bit	Bit Definition	Bit Value	Value Definition
31:0	FRC weight. These registers specify FRC weights. The FRC utility will be provided to change this data.		

The bits in this register select the corresponding first 32 flat panel PWM clock pulses (0 to 31) to generate the FPWMCLK output signal.

Register 4-77: Flat-Panel PWM Clock Selector (FP32R: Index C8h, Offset 6C8h)

Bit	Bit Definition	Bit Value	Value Definition
31:0	Flat panel PWM Clock Select A 1 in any of the bits in this register sets the corresponding flat panel PWM clock pulse on FPWMCLK. A 0 in any of the bits in this register ensures that the corresponding flat panel PWM clock pulse is not generated on FPWMCLK.		

The bits in this register select the corresponding second 32 flat panel PWM clock pulses (32 to 63) to generate the FPWMCLK output signal.

Register 4-78: Flat-Panel PWM Clock Selector (FP33R: Index CCh, Offset 6CCh)

Bit	Bit Definition	Bit Value	Value Definition
31:0	Flat panel PWM Clock Select A 1 in any of the bits in this register sets the corresponding flat panel PWM clock pulse on FPWMCLK. A 0 in any of the bits in this register ensures that the corresponding flat panel PWM clock pulse is not generated on FPWMCLK.		

The bits in this register select the corresponding third 32 flat panel PWM clock pulses (64 to 95) to generate the FPWMCLK output signal.

Register 4-79: Flat-Panel PWM Clock Selector (FP34R: Index D0h, Offset 6D0h)

Bit	Bit Definition	Bit Value	Value Definition
31:0	Flat panel PWM Clock Select A 1 in any of the bits in this register sets the corresponding flat panel PWM clock pulse on FPWMCLK. A 0 in any of the bits in this register ensures that the corresponding flat panel PWM clock pulse is not generated on FPWMCLK.		

The bits in this register select the corresponding fourth 32 flat panel PWM clock pulses (96 to 127) to generate FPWMCLK Output signal. If there are more than 128 PWM clock pulses, the remaining clock pulses will not be output on the FPWMCLK pin.

Register 4-80: Flat-Panel PWM Clock Selector (FP35R: Index D4h, Offset 6D4h)

Bit	Bit Definition	Bit Value	Value Definition
31:0	Flat panel PWM Clock Select A 1 in any of the bits in this register sets the corresponding flat panel PWM clock pulse on FPWMCLK. A 0 in any of the bits in this register ensures that the corresponding flat panel PWM clock pulse is not generated on FPWMCLK.		

Register 4-81: FRC Weight (FP36R: Index D8h, Offset 6D8h)

Bit	Bit Definition	Bit Value	Value Definition
31:0	FRC weight. These registers specify FRC weights. The FRC utility will be provided to change this data.		

Register 4-82: FRC Weight (FP37R: Index 0DCh, Offset 6DCh)

Bit	Bit Definition	Bit Value	Value Definition
31:0	FRC weight. These registers specify FRC weights. The FRC utility will be provided to change this data.		

Note: *Depending on the CPU interface used, the mapping of the FP30-FP37R is different. For the Motorola Dragonball and PCI interfaces, the mapping is as described above. For the SA-11xx, NEC 41xx and Hitachi 77xx processors, the registers need to be accessed differently, as follows:*

FP30R-FP37R (index C0h-DCh) Mapped to FP70R-FP77R (Index 1C0h-1DCh)

4.11 Graphics Engine Programming

The MQ-1100/1132 graphics engine comprehensively supports various BitBLT operations, including all 256 ROPs. The graphics engine also implements a full Bresenham line-draw algorithm which enables any arbitrary angle line draw in hardware. *Figure 4-5* outlines the address space for the graphics engine registers and describes the register set in detail.

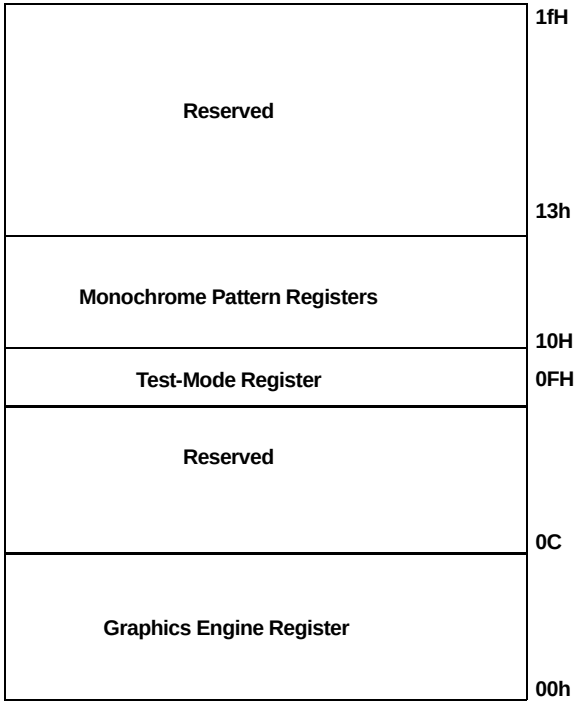


Figure 4-5. Address Space for Graphics Engine Registers

4.11.1. Graphics Engine Module Register Set List

The registers included in this list are necessary to create the graphic engine module:

4.11.2. Graphics Engine Register Definition

Register 4-11 specifies the index, offset and reset values for the graphics engine registers.

TABLE 4-11: Graphics Engine Register Index and Reset Values

Register	Index	Offset	Reset Value	See Description
GE00R	00h	200h	0000-0000h	*Register 4-83 on page 133*
GE01R	04h	204h	xxxx-xxxxh	*Register 4-84 on page 135, Register 4-85 on page 135*
GE02R	08h	208h	xxxx-xxxxh	*Register 4-86 on page 136, Register 4-87 on page 136*
GE03R	0Ch	20Ch	xxxx-xxxxh	*Register 4-88 on page 137, Register 4-89 on page 137*
GE04R	10h	210h	xxxx-xxxxh	*Register 4-90 on page 137*
GE05R	14h	214h	xxxx-xxxxh	*Register 4-91 on page 137*
GE06R	18h	218h	xxxx-xxxxh	*Register 4-92 on page 138*
GE07R	1Ch	21Ch	xxxx-xxxxh	*Register 4-93 on page 138*
GE08R	20h	220h	xxxx-xxxxh	*Register 4-94 on page 138*
GE09R	24h	224h	xxxx-xxxxh	*Register 4-95 on page 139, Register 4-96 on page 139*
GE0AR	28h	228h	xxxx-xxxxh	*Register 4-97 on page 140*
GE0BR	2Ch	22Ch	xxxx-xxxxh	*Register 4-98 on page 141*
GE0CR	30h	230h	0000-0000h	*Register 4-99 on page 141*
GE0FR	3Ch	23Ch	xxxx-xxxxh	*Register 4-100 on page 142, Register 4-101 on page 142, Register 4-102 on page 142, Register 4-103 on page 143*
GE10R	40h	240h	xxxx-xxxxh	*Register 4-104 on page 143*
GE11R	44h	244h	xxxx-xxxxh	*Register 4-105 on page 143*
GE12R	48h	248h	xxxx-xxxxh	*Register 4-106 on page 143*
GE13R	4Ch	24Ch	xxxx-xxxxh	*Register 4-107 on page 144*

Register 4-83: Drawing Command Register (GE00R: Index 00h, Offset 200h)

Bit	Bit Definition	Bit Value	Value Definition
7:0	Raster Operation (ROP) This defines the 8-bit ROP. All 256 possible ROPs are supported.		
10:8	Command Type These bits define the supported drawing commands.	000	NOP No Operation.
		010	BitBLT A rectangle of defined location, height and width is transferred to another location in memory. Source memory is defined by bit 13 of this register. Display-memory to display-memory and system-memory to display-memory. BLT are supported. The logic supports a 3-operand (pattern, source, destination) raster engine so that all 256 ROPs specified in bits [7:0] are supported. Monochrome source and/or monochrome pattern can also be supported.
		011	Reserved
		100	Line Draw
		101	Reserved
		111	Reserved
11	X Direction This bit defines the direction of transfer for the X coordinate. This bit must be set to 0 for a monochrome source.	0	Positive X direction (left-to-right drawing direction). X coordinates for source and destination width counters and the address registers within a line get increminated after transfer of each pixel.
		1	Negative X direction (right-to-left drawing direction). X coordinates for source and destination width counters and the address registers within a line get decremented after transfer of each pixel.

Register 4-83: Drawing Command Register (GE00R: Index 00h, Offset 200h)

Bit	Bit Definition	Bit Value	Value Definition
12	Y Direction This bit defines the direction of transfer for the Y coordinate.	0	Positive Y direction (top-to-bottom drawing direction). Height counters and address registers for source and destination get incremi-nated after transfer of each line.
		1	Negative Y direction (bottom-to-top drawing direction). Height counters and address registers, for source and destination get decre-mented after transfer of each line.
13	Source Memory This bit defines the source memory for Bit-BLT operation. Source data can come from either screen (display memory) or from memory (system memory).	0	Source window is in screen.
		1	Source window is in the system memory. CPU must write source data to the source FIFO.
14	Monochrome source This bit specifies whether source data is monochrome (1 bpp) or color.	0	Color source. Source data has the same color depth as destination data.
		1	Monochrome source. Source data is 1 bpp and will be expanded to the value stored in either the foreground or background color regis-ters.
15	Monochrome Pattern Must be programmed to 1	0	Monochrome pattern is disabled.
		1	Monochrome pattern.
16	Color Transparency Enable Setting this bit enables transparency depend-ing on destination (output) color data.	0	Destination transparency is disabled.
		1	Destination transparency is enabled. The output result of the raster operation is compared with the color compare registers and the trans-parency depends on bit 17.
17	Destination Transparency Polarity This bit defines polarity for destination trans-parency.	0	Destination data is not updated (transparent) if this data is equal to the color compare register value.
		1	Destination data is not updated (transparent) if this data is not equal to color compare register value.
18	Monochrome Source or Monochrome Pattern Transparency Enable This bit enables transparency depending on monochrome pattern data (bit 15 is set) or monochrome source data (bit 14 is set).	0	Monochrome transparency is disabled.
		1	Monochrome source or monochrome pattern transparency is enabled. Either foreground color or background color is defined as transparent depending on bit 19.
19	Monochrome Transparency Polarity This bit defines polarity for monochrome pattern transparency.	0	Background color for monochrome source or monochrome pattern is transparent.
		1	Foreground color for monochrome source or monochrome pattern is transparent.
20	Memory to screen or off screen to screen mode select.	0	Use lined mode definition in GE09R.
		1	Use packed mode definition in register GE09R.
22:21	Reserved.		
23	Solid source color Setting this bit forces all source data to fore-ground color if monochrome source bit is set.	0	source data is specified by contents of source FIFO.
		1	Solid color. All source data is forced to the value of Foreground Color register (GE07R).
24	Source stride is equal to destination stride	0	Source stride is equal to destination stride, GE09R[11:0] is ignored
		1	Source stride is not equal to destination stride, GE09R[11:0] has to be programmed
25	ROP2 Code selection	0	The ROP code is [7:0]
		1	The ROP code is ROP2. Therefore, [3:0] is duplicated to [7:4].

Register 4-83: Drawing Command Register (GE00R: Index 00h, Offset 200h)

Bit	Bit Definition	Bit Value	Value Definition
26	Enable Clipping Setting this bit enables clipping. Clipping area is defined as a rectangle. Destination (output) pixels outside the clipping rectangle are not written to the destination.	0	Clipping is disabled.
		1	Clipping is enabled.
27	Auto Execute Setting this bit enables auto-execution of 2D command after the destination XY register is written.	0	The graphics engine command execution starts after this register is written.
		1	The graphics engine command execution starts after the destination XY register is written.
29:28	Reserved.		
30	Solid pattern Setting this bit forces all pattern data to foreground color.	0	The pattern registers specify the pattern data.
		1	All pattern data is forced to the value of the pattern foreground color register (GE12R).
31	Color transparency compare source	0	The color transparency is compare against source data.
		1	The color transparency is compare against destination read data (blue screen effect).

Register GE01R is for both BitBLT and line draw. *Register 4-84* lists the register definitions for BitBLT, and *Register 4-85* lists the definitions for Bresenham line draw.

Register 4-84: BitBLT Width and Height Parameter Register (GE01R: Index 04h, Offset 204h)

Bit	Bit Definition	Bit Value	Value Definition
11:0	Source or Destination Window Width This parameter defines the number of pixels in each source or destination line.		
15:12	Reserved		
27:16	Source or Destination Window Height This parameter defines the number of lines in the source or destination window.		
30:28	Reserved		
31	Enable starting XY conversion according to XY direction.	0	Starting XY is the calculated value according to XY direction.
		1	Always put the left, top corner as the starting XY and let hardware to calculate the final XY according to the direction of XY (bit 11 and bit 12 of GE00R)

Register 4-85: Bresenham Line Draw Parameter Register (GE01R: Index 04h, Offset 204h)

Bit	Bit Definition	Bit Value	Value Definition
16:0	This value is either –(dm >>1) – 1 or –(dm >> 1), depending on the quadrant. Since it is always a negative value, it is 2's complement value in this register.		
28:17	Length along the major-axis height. If it is x major, this is the width of the line; if it is y major, this is the height of the line		
29	x-major or y-major	0	x-major
		1	y-major

Register 4-85: Bresenham Line Draw Parameter Register (GE01R: Index 04h, Offset 204h)

Bit	Bit Definition	Bit Value	Value Definition
30	Decision to draw or not to draw the last pixel of the line	0	Always draw the last pixel of the line (the length along the major axis in[28:17])
		1	Not to draw the last pixel of the line (the length along the major axis in [28:17] – 1)
31	Enable to use quadrant number instead of X, Y, direction in drawing command register.	0	Use quadrant GE02R[31:29] to decide the major and XY direction
		1	Use bit 29 in this register to decide major and bit 11 and bit 12 of GE00R to decide XY direction.

Register GE02R defines the X and Y starting position of the destination window or line draw starting XY. *Register 4-86* specifies the register definitions for the X and Y starting position of the destination window. *Register 4-87* specifies the definitions for the line draw starting XY.

Register 4-86: Destination XY Resister (GE02R: Index 08h, Offset 208h)

Bit	Bit Definition	Bit Value	Value Definition
11:0	Destination X Position This parameter defines the X start position of destination window.		
12	Reserved		
15:13	Monochrome Pattern Horizontal Offset This parameter is used to indicate starting pixel for monochrome or color pattern data for each line of pattern data.	000	Pattern data line starts at pixel 0.
		001	Pattern data line starts at pixel 1.
		010	Pattern data line starts at pixel 2.
		011	Pattern data line starts at pixel 3.
		100	Pattern data line starts at pixel 4.
		101	Pattern data line starts at pixel 5.
		110	Pattern data line starts at pixel 6.
		111	Pattern data line starts at pixel 7.
27:16	Destination Y Position This parameter defines the Y start position of destination window.		
28	Reserved		
31:29	Monochrome Pattern Vertical Offset This parameter is used to indicate starting line for monochrome pattern data.	000	Pattern data starts from line 0.
		001	Pattern data starts from line 1.
		010	Pattern data starts from line 2.
		011	Pattern data starts from line 3.
		100	Pattern data starts from line 4.
		101	Pattern data starts from line 5.
		110	Pattern data starts from line 6.
		111	Pattern data starts from line 7.

Register 4-87: Line Draw Starting X Coordinate and Major Axis Delta (GE02R: Index 08h, Offset 208h)

Bit	Bit Definition	Bit Value	Value Definition
11:0	Starting X coordinate. This parameter defines the x start point of line draw.		
28:12	17 bits major-axis delta (dm).		
31:29	Quadrant number	000	Quadrant 0 (x-major, positive x and y directions)
		001	Quadrant 1 (y-major, positive x and y directions)
		010	Quadrant 2 (y-major, negative x and positive y directions)
		011	Quadrant 3 (x-major, negative x and positive y directions)
		100	Quadrant 4 (x-major, negative x and y directions)
		101	Quadrant 5 (y-major, negative x and y directions)
		110	Quadrant 6 (y-major, positive x and negative y directions)
		111	Quadrant 7 (x-major, positive x and negative y directions)

Register GE03R defines the X and Y starting position of the source window, or, in line draw, it defines delta in major and minor axis and the four least significant bits (LSBs) are fraction bits for precision. *Register 4-88* specifies the X and Y starting position, and *Register 4-89* defines delta in major and minor axis.

Register 4-88: Source XY Register (GE03R: Index 0Ch, Offset 20Ch)

Bit	Bit Definition	Bit Value	Value Definition
11:0	Source X Position This parameter defines the X start position of source window.		
15:12	Reserved		
27:16	Source Y Position This parameter defines the Y start position of source window.		
31:28	Reserved		

Register 4-89: Line Draw Starting Y Coordinate and Minor Axis Delta (GE03R: Index 0Ch, Offset 20Ch)

Bit	Bit Definition	Bit Value	Value Definition
11:0	Starting Y coordinate		This parameter defines the y-start position of line draw.
28:12	17 bits minor-axis delta (dn).		
31:29	Reserved.		

Register GE04R determines the destination or source (depending on GE00R[31]) color for destination color transparency.

Register 4-90: Color Compare Register (GE04R: Index 10h, Offset 210h)

Bit	Bit Definition	Bit Value	Value Definition
15:0	Destination Transparent Color This is an 8- or 16-bpp color for destination color transparency.		
31:16	Reserved		

Register GE05R specifies the left edge and the top edge of the clipping window. All destination (output) pixels outside the clipping rectangle are clipped.

Register 4-91: Clip Left/Top Register (GE05R: Index 14h, Offset 214h)

Bit	Bit Definition	Bit Value	Value Definition
10:0	Left Edge of Clipping Rectangle This parameters specify the left edge of the clipping rectangle. All destination (output) pixels with X coordinates less than this value are not written.		
15:11	Reserved		
25:16	Top Edge of Clipping Rectangle This parameters specify the top edge of the clipping rectangle. All destination (output) pixel with Y coordinate less than this value will not be written.		
31:26	Reserved		

Register GE06R specifies the right edge and bottom edge of the clipping window. All destination (output) pixels outside the clipping reacting are clipped.

Register 4-92: Clip Right/Bottom Register (GE06R: Index 18h, Offset 218h)

Bit	Bit Definition	Bit Value	Value Definition
10:0	Right Edge of Clipping Rectangle This parameter specifies the right edge of the clipping rectangle. All destination (output) pixels with X coordinates larger than this value are not written.		
15:11	Reserved		
25:16	Bottom Edge of Clipping Rectangle This parameters specify the bottom edge of the clipping rectangle. All destination (output) pixel with Y coordinate larger than this value will not be written.		
31:26	Reserved		

Register GE07R defines the non-transparent foreground color when a monochrome source is set.

Register 4-93: Foreground Color Register for Monochrome Source (GE07R: Index 1Ch, Offset 21Ch)

Bit	Bit Definition	Bit Value	Value Definition
15:0	Foreground Color This is an 8- or 16-bpp foreground color value. Bits [7:0] are used for 8-bpp mode. Bits [15:0] are used for 16-bpp mode.		
31:16	Reserved		

Register GE08R defines the non-transparent background color when monochrome source is reset.

Register 4-94: Background Color Register (GE08R: Index 20h, Offset 220h)

Bit	Bit Definition	Bit Value	Value Definition
15:0	Background Color This is an 8- or 16-bpp background color value. Bits [7:0] are used for 8-bpp mode. Bits [15:0] are used for 16-bpp mode.		
31:16	Reserved		

Register GE09R defines the stride and offset for source line. There are two different definitions for the source line depending on whether you are in lined mode or packed mode. Lined mode (see *Register 4-95*) needs stride and initial offset. For a monochrome source, you also need a bit and byte offset. For a color source, you also need a byte offset. It is the programmer's responsibility to write dummy write to the source FIFO if the stride is less than 8 bytes. Packed mode set-up can occur at both the monochrome source and the color source (see *Register 4-96*). For a monochrome source, it needs initial byte and bit offset and subsequent byte and bit space. For off-screen to on-screen BitBLT, it also needs amount of 64 bits pass to MIU. For color source, the space is always in byte boundary.

Register 4-95: Source Stride Register (GE09R: Index 24h, Offset 224h)

Bit	Bit Definition	Bit Value	Value Definition
9:0	Source Line Stride This parameter specifies the number of bytes from the first pixel of a source line to the first pixel of the next source line when a monochrome or color source data comes from screen (display memory). Destination line stride is used instead of this parameter to calculate the address of the first pixel of a monochrome or color source window when the source comes from screen.		
24:10	Reserved		
27:25	These bits are reserved in display-memory to display-memory BitBLT. But for monochrome to on screen lined mode, these three bits are for bits offset for the first pixel of each line.	000	Monochrome source starts at bit 0.
		001	Monochrome source starts at bit 1.
		010	Monochrome source starts at bit 2.
		011	Monochrome source starts at bit 3.
		100	Monochrome source starts at bit 4.
		101	Monochrome source starts at bit 5.
		110	Monochrome source starts at bit 6.
		111	Monochrome source starts at bit 7.
30:28	These bits are reserved for display-memory to display-memory BitBLT. But for a color source system to screen BitBLT, these three bits are for byte offset of the first line. For monochrome source off screen to on screen lined mode, this is the byte offset for initial line.	000	Monochrome or color source line starts at byte 0.
		001	Monochrome or color source line starts at byte 1.
		010	Monochrome or color source line starts at byte 2.
		011	Monochrome or color source line starts at byte 3.
		100	Monochrome or color source line starts at byte 4.
		101	Monochrome or color source line starts at byte 5.
		110	Monochrome or color source line starts at byte 6.
		111	Monochrome or color source line starts at byte 7.
31	Reserved.		

Register 4-96: Pack Mode Set-up (GE09R: Index 24h, Offset 224h)

Bit	Bit Definition	Bit Value	Value Definition
2:0	Initial Monochrome Source Bit Offset This parameter indicates the starting bit offset for the first line of a monochrome source from either memory or screen. For a color source, set these bits to zero.	000	Monochrome source line starts at bit 0.
		001	Monochrome source line starts at bit 1.
		010	Monochrome source line starts at bit 2.
		011	Monochrome source line starts at bit 3.
		100	Monochrome source line starts at bit 4.
		101	Monochrome source line starts at bit 5.
		110	Monochrome source line starts at bit 6.
		111	Monochrome source line starts at bit 7.

Register 4-96: Pack Mode Set-up (GE09R: Index 24h, Offset 224h)

Bit	Bit Definition	Bit Value	Value Definition
5:3	Initial Monochrome or Color Source Byte Offset This parameter indicates the starting byte for the first line of monochrome source data from system memory or the initial byte offset for monochrome off-screen source data.	000	Monochrome or color source line starts at byte 0.
		001	Monochrome or color source line starts at byte 1.
		010	Monochrome or color source line starts at byte 2.
		011	Monochrome or color source line starts at byte 3.
		100	Monochrome or color source line starts at byte 4.
		101	Monochrome or color source line starts at byte 5.
		110	Monochrome or color source line starts at byte 6.
		111	Monochrome or color source line starts at byte 7.
15:6	Number of 8 bytes amount that MIU needs to fetch from frame buffer. For off-screen to on-screen packed mode, these 10 bits represent the number of 8 bytes needed to be fetched by the MIU; the maximum amount it can address is 16 Kbyte, which is the off screen monochrome font or monochrome image graphics engine can support for packed mode.		
24:16	Reserved		
27:25	Bit Space between lines For system to screen or off-screen to screen BitBLT, these bits are used for bit space between lines. For a color source, set these bits to zero. The graphics engine uses these bits and concatenate with byte space (bits [31:28]) to calculate the total bit space for packmode. Therefore if it is monochrome source, bit [31:25] becomes total bit space between two line. If it is color source, the byte space is programmed into bit [31:28].		
31:28	Byte space between lines This parameter is used to indicate the byte space between the end of the first line and the beginning of the next line.		

Register GE0AR is the destination stride and color depth register, usually only programmed once.

Register 4-97: Destination Stride Register and Color Depth (GE0AR: Index 28h, Offset 228h)

Bit	Bit Definition	Bit Value	Value Definition
9:0	Destination Line Stride This parameter specifies the number of bytes from the first pixel of a line to the first pixel of the next line for destination data. This parameter is also used to calculate the address of the first pixel of destination window and the first pixel of mono/color source window if source comes from screen (display memory). For clipping, the destination stride has to be on the 8 bytes (64 bits) boundary, the least significant four bits are always zero.		
27:10	Reserved		

Register 4-97: Destination Stride Register and Color Depth (GE0AR: Index 28h, Offset 228h)

Bit	Bit Definition	Bit Value	Value Definition
28	Bit swap for mono source data	0	Pixel 0 is in the MSB of the byte: such as Windows CE and Palm
		1	Pixel 0 is in the LSB of the byte. Pixel 7 is in the MSB of the byte: such as EPOC.
29	Enable 90° clockwise rotation (i.e., the OS managing the window is based on the counter clockwise data).	0	Graphics engine rendering graphics is according to 0° rotation (no rotation).
		1	Graphics engine rendering graphics is according to 90° rotation.
31:30	Color Depth This parameter defines the destination data and for color source or pattern bpp.	00	8 bpp.
		01	16 bpp.
		1X	Reserved

Register GE0BR is the base (start) address of the image in the display memory.

Register 4-98: Base Address Register (GE0BR: Index 2Ch, Offset 22Ch)

Bit	Bit Definition	Bit Value	Value Definition
19:0	Base Address This parameter defines the start address of the image in the display memory. This is byte address but the lower 3 bits are internally forced to zeros therefore this parameter is aligned to 64 bits boundary. During the register read, always read the bits 19-3, because the LSB three bits are not implemented.		
28:20	Reserved		
29	Test Mode Enable. Setting this bit enables test mode, allowing the internal ALU to be read through register GE0FR. This bit is used for factory testing only.	0	Test mode disabled.
		1	Test mode enabled.
31:30	Test Mode Control These bits are used when test mode is enabled.	00	The address calculation results appear in register GE0FR.
		01	The clipping left and right results appear in register GE0FR.
		10	The clipping top and bottom results appear in register GE0FR.
		11	The state machine status appears in register GE0FR

Register GE0CR has two functions: to specify the command start window, which specifies when the current graphics engine command can start, and to instruct the graphics controller to switch between main and alternate windows.

Register 4-99: Graphics Engine Command Start Control Register (GE0CR: Index 30h, Offset 230h)

Bit	Bit Definition	Bit Value	Value Definition
9:0	Command start window beginning line number This parameter specifies the line number where the command start window begins.		
11:10	Reserved		
21:12	Command start window ending line number This parameter specifies the line number where the command start window ends. (Note:)		
23:22	Reserved		

Register 4-99: Graphics Engine Command Start Control Register (GE0CR: Index 30h, Offset 230h)

Bit	Bit Definition	Bit Value	Value Definition
24	Command Start Window Control This parameter specifies whether the command start window must check with the graphics controller before executing a command.	0	Command is executed immediately.
		1	Command execution starts when the graphics controller vertical counter is in the command start window.
25	Reserved		
27:26	GC1 Switching Window Control This parameter controls double buffering for GC1.	x0	Do not send a signal to the graphics controller to the switch buffer at the end of the current command.
		01	Send a signal to GC to switch to the main window buffer at the end of the current command.
		11	Send a signal to GC to switch to alternate window buffer at the end of the current command.
31:28	Reserved		

Note: *The command start window ending line number is not necessarily smaller than the command start window beginning line number.*

Register GE0FR is a read-only register which can be used to read internal status in test mode. If test mode is disabled, this register returns an unpredictable value. Register GE0FR is available for address calculation results (see *Register 4-100*), clipping left and right results (see *Register 4-101*), clipping top and bottom results (see *Register 4-102*), and state machine results (see *Register 4-103*).

Register 4-100: Test Mode Address Calculation (GE0FR: Index 3Ch, Offset 23Ch)

Bit	Bit Definition	Bit Value	Value Definition
20:0	GEOBR [31:30] are set to 00. This contains the source address results from the ALU.		
31:21	Reserved. Must be programmed to 0.		

Register 4-101: Test Mode Clipping Left and Right (GE0FR: Index 3Ch, Offset 23Ch)

Bit	Bit Definition	Bit Value	Value Definition
8:0	GEOBR [31:30] are set to 01. This contains the left difference between shcleft and shdstx.		
15:9	Reserved. Must be programmed to 0.		
24:16	Containing the right difference between shcright and shdstx.		
31:25	Reserved. Must be programmed to 0.		

Register 4-102: Test Mode Clipping Top and Bottom (GE0FR: Index 3Ch, Offset 23Ch)

Bit	Bit Definition	Bit Value	Value Definition
11:0	GEOBR [31:30] are set to 11. This contains the top difference between shctop and shdsty.		
15:12	Reserved. Must be programmed to 0.		
27:16	It contains the bottom difference between shcbot and shdsty.		
31:28	Reserved. Must be programmed to 0.		

Register 4-103: Test Mode State Machine (GE0FR: Index 3Ch, Offset 23Ch)

Bit	Bit Definition	Bit Value	Value Definition
2:0	Command read state machine status.		
6:3	Pipeline control state machine status.		
31:7	Reserved. Must be programmed to 0.		

Registers GE10R and GE11R contain the first four and second four lines of monochrome-pattern data, respectively.

Register 4-104: Monochrome Pattern Register 0 (GE10R: Index 40h, Offset 240h)

Bit	Bit Definition	Bit Value	Value Definition
7:0	Line 0 of monochrome pattern. Pixel 0 is the most significant bit and pixel 7 is the least significant bit.		
15:8	Line 1 of monochrome pattern. Pixel 0 is the most significant bit and pixel 7 is the least significant bit.		
23:16	Line 2 of monochrome pattern. Pixel 0 is the most significant bit and pixel 7 is the least significant bit.		
31:24	Line 3 of monochrome pattern. Pixel 0 is the most significant bit and pixel 7 is the least significant bit.		

Register 4-105: Monochrome Pattern Register 1 (GE11R: Index 44h, Offset 244h)

Bit	Bit Definition	Bit Value	Value Definition
7:0	Line 4 of monochrome pattern. Pixel 0 is the most significant bit and pixel 7 is the least significant bit.		
15:8	Line 5 of monochrome pattern. Pixel 0 is the most significant bit and pixel 7 is the least significant bit.		
23:16	Line 6 of monochrome pattern. Pixel 0 is the most significant bit and pixel 7 is the least significant bit.		
31:24	Line 7 of monochrome pattern. Pixel 0 is the most significant bit and pixel 7 is the least significant bit.		

Register GE12R defines the non-transparent foreground color when the monochrome pattern is set.

Register 4-106: Pattern Foreground Color Register (GE12R: Index 48h, Offset 248h)

Bit	Bit Definition	Bit Value	Value Definition
15:0	Foreground Color This is the 8- or 16-bpp foreground color value. Bits [7:0] are used for 8-bpp mode. Bits [15:0] are used for the 16 bpp mode.		
31:16	Reserved		

Register GE13R defines the non-transparent background color when the monochrome pattern is 0.

Register 4-107: Pattern Background Color Register (GE13R: Index 4Ch, Offset 24Ch)

Bit	Bit Definition	Bit Value	Value Definition
15:0	Background Color This is the 8- or 16-bpp background color value. Bits [7:0] are used for 8-bpp mode. Bits [15:0] are used for the 16 bpp mode.		
31:16	Reserved		

You can implement either rectangle fill or line draw in a monochrome source BitBLT or monochrome pattern BitBLT. If implemented in a source BitBLT, set the monochrome source and solid color bit in the drawing command register. If implemented in a pattern BitBLT, set the monochrome pattern and solid color bit.

For off-screen to screen BitBLT, if the source stride is not in the quad word boundary (64 bits boundary), then the monochrome screen to screen BitBLT can only be done for four lines (in the line mode). During hardware rotation support, the stride is in word boundary. If the initial offset for monochrome source data falls into quad word boundary, then every four lines, there is one quad word needs to be skipped. The MIU does not have this information, so the solution is to do the monochrome screen to screen BitBLT every four lines.

4.12 USB Function

The USB function is designed to operate at full speed (12 Mbps). It supports five end points, each of which can be individually activated.

Table 4-12 specifies the index and reset values for the USB registers.

TABLE 4-12: USB Register Index and Reset Values

Register	Index	Offset	Reset Value	See Description
UD00R	00h	1000h	0000-0000h	*Register 4-108 on page 145*
UD01R	04h	1004h	0000-0000h	*Register 4-109 on page 147*
UD02R	08h	1008h	0000-0000h	*Register 4-110 on page 147*
UD03R	0Ch	100Ch	0000-0000h	*Register 4-111 on page 148*
UD04R	10h	1010h	0000-0000h	*Register 4-112 on page 149*
UD05R	14h	1014h	0000-0000h	*Register 4-113 on page 150*
UD06R	18h	1018h	0000-0000h	*Register 4-114 on page 150*
UD07R	1Ch	101Ch	0000-0000h	*Register 4-115 on page 151*
UD08R	20h	1020h	0000-0000h	*Register 4-116 on page 151*
UD09R	24h	1024h	0000-0000h	*Register 4-117 on page 151*
UD0AR	28h	1028h	0000-0000h	*Register 4-118 on page 152*
UD0BR	2Ch	102Ch	xxxx-xx00h	*Register 4-119 on page 153*
UD0CR	30h	1030h	0000-0000h	*Register 4-120 on page 154*
UD0DR	34h	1034h	0000-0000h	*Register 4-121 on page 155*
UD0ER	38h	1038h	0000-0000h	*Register 4-122 on page 155*
UD0FR	3Ch	103Ch	0000-0000h	*Register 4-123 on page 157*
UD10R	40h	1040h	0000-0000h	*Register 4-124 on page 158*
UD11R	44h	1044h	0000-0000h	*Register 4-125 on page 160*
UD12R	48h	1048h	0000-0000h	*Register 4-126 on page 160*

Register 4-108 through *Register 4-126*, specifies the USB register bit values and definitions. Register UD00R is a read/write register.

Register 4-108: USB Function General Control Register 1 (Read/Write) Register (UD00R: Index 00h, Offset 1000h)

Bit	Bit Definition	Bit Value	Value Definition
0	Suspend Detection Enable This bit allows the clocks to shutdown in low power mode.	0	Suspend Detection is enabled
		1	Suspend Enable
2:1	Reserved.		
3	Remote Host wakeup Enable Setting this bit allows the device to wakeup the suspended host if necessary.	0	Remote Host Wakeup disable
		1	Remote Host Wakeup Enable
4	Reserved.		
5	End Point 2 Bulk or ISO This bit determines whether Endpoint 2 is a bulk or isochronous endpoint. This bit must be written as soon as USB reset is detected.	0	EP2 is a bulk endpoint.
		1	EP2 is isochronous endpoint.
6	End Point 3 Bulk or ISO This bit determines whether Endpoint 3 is a bulk or isochronous endpoint. This bit must be written as soon as USB reset is detected.	0	EP3 is bulk endpoint.
		1	EP3 is isochronous endpoint.
7	Reserved		

Register 4-108: USB Function General Control Register 1 (Read/Write) Register (UD00R: Index 00h, Offset 1000h)

Bit	Bit Definition	Bit Value	Value Definition
8	Wakeup USB Host. Software must set this bit for the device to wakeup the remote USB host. This generates a wakeup pulse in the hardware, which is sent to Suspend. Wakeup logic. This bit is valid if only the remote HOST wakeup enable feature is enabled. (UD00R[3]).	0	Disable wakeup.
		1	Wakes up the remote USB Host.
15:9	Reserved		
16	Start Of Frame Interrupt Enable (SOFIEN) This bit enables the generation of interrupt due to start of frame (SOF) recognition or recognition of any errors relating to SOF (frame number register).	0	Disable interrupt.
		1	Enable interrupt.
17	End Point 0 Tx Interrupt Enable (EP0RIEN) This bit enables the generation of an interrupt due to the completion of a transfer on end point 0 Tx.	0	Disable interrupt.
		1	Enable interrupt.
18	End Point 0 Rx Interrupt Enable (EP0TIEN) This bit enables the generation of an interrupt due to the completion of a transfer on end point 0 Rx.	0	Disable interrupt.
		1	Enable interrupt.
19	End Point 1 Tx Interrupt Enable(EP1TIEN) This bit enables the generation of an interrupt due to the completion of a transfer on end point 1 Tx.	0	Disable interrupt.
		1	Enable interrupt.
20	End Point 2 Tx EOT Interrupt Enable This bit enables the generation of an interrupt due to the end of a transaction on end point 2 Tx.	0	Disable interrupt.
		1	Enable interrupt.
21	End Point 3 Rx EOT Interrupt Enable This bit enables the generation of an interrupt due to the end of a transaction on end point 3 Rx.	0	Disable interrupt.
		1	Enable interrupt.
22	Interrupt enable for the DMA Transmit to interrupt every time the end of the transmit buffer is reached. If this bit is set, it enables the interrupt to the CPU every time the transmit buffer end in the EDRAM is reached.	0	Disable interrupt.
		1	Enable interrupt.
23	Interrupt enable for the DMA Receive to interrupt every time the receive buffer end is reached. If this bit is set, it allows the CPU interrupt to empty the receive buffer in the internal memory. An interrupt is generated every time the DMA controller writes cross the buffer boundary.	0	Disable interrupt.
		1	Enable interrupt.

Register 4-108: USB Function General Control Register 1 (Read/Write) Register (UD00R: Index 00h, Offset 1000h)

Bit	Bit Definition	Bit Value	Value Definition
24	Interrupt enable for the DMA Receive at the end of transfer. If this bit is set, it allows the CPU interrupt to empty the remaining data in the receive buffer in the internal memory. The received data may not be a multiple of the buffer size. Therefore, at the end of the transfer, the CPU should be interrupted to transfer the last data. The end of the transfer is detected when the device receives a zero-length packet or a short packet.	0	Disable interrupt.
		1	Enable interrupt.
25	Interrupt Enable for Global Suspend If this bit is set, it enables the interrupt to the CPU when the USB device logic goes into global suspend mode.	0	Disable interrupt.
		1	Enable interrupt.
26	Interrupt Enable for Wakeup If this bit is set, it enables the interrupt to the CPU when the USB device logic detects wakeup signaling coming from host.	0	Disable interrupt.
		1	Enable interrupt.
27	Reset signaling Interrupt Enable	0	Disable interrupt.
		1	Enable interrupt.
31:28	Reserved		

Register UD01R is a read/write address register (see *Register 4-109*). When this register is reset, it is set to the value 0000h. After enumeration, the CPU writes the device address, assigned by the host, into this register. This address is used for address matching for the addresses coming on the USB data lines. The whole function has only one USB device address.

Register 4-109: USB Function Address Register (UD01R: Index 04h, Offset 1004h)

Bit	Bit Definition	Bit Value	Value Definition
6:0	USB Device Address (UAR) This is set to the value obtained after the enumeration process. Software must write the device address to this.		
31:7	Reserved		

Register UD02R is a read-only register (see *Register 4-110*). It cannot be cleared. After enumeration, the USB writes the current frame number at each SOF token.

Register 4-110: USB Function Frame Number Register (UD02R: Index 08h, Offset 1008h)

Bit	Bit Definition	Bit Value	Value Definition
10:0	USB Frame Number This is set to the value obtained after the SOF token is received. Only S/W can read this value.		
11	Frame Number Corrupted (FNC) This bit is set if the current received frame number is corrupted.		
12	New Frame (NF) This bit is set when a new frame is received.		

Register 4-110: USB Function Frame Number Register (UD02R: Index 08h, Offset 1008h)

Bit	Bit Definition	Bit Value	Value Definition
13	Missing Frame (MF) – Valid only if EP2 or EP3 is configured as ISO This bit is set whenever a SOF is missing between two consecutive ISO packets.		
14	Missing Data (MD) for EP2 – Valid only if EP2 is configured as ISO This bit is set whenever a packet is missing between two consecutive SOFs.		
15	Missing Data (MD) for EP3 – Valid only if EP3 is configured as ISO This bit is set whenever a packet is missing between two consecutive SOFs.		
31:16	Reserved		

Register UD03R is the read/write control register for Transmit endpoint 0 (see *Register 4-111*).

Register 4-111: End Point 0 Transmit Control Register (UD03R: Index 0Ch, Offset 100Ch)

Bit	Bit Definition	Bit Value	Value Definition
0	Reserved (R/W)		
1	End Of Data Transmit (EDT) This bit if set indicates that the last byte of the data transmission is written into the FIFO. Software sets this bit after loading the last Dword into the FIFO. Hardware clears this bit after the last byte is transmitted and ACKd.		
2	Send A Stall (SAS) This bit indicates that the function should send a STALL to the host. If this bit is asserted at least one clk12 cycle before valid_token goes active for this transaction, then the transaction is stalled. If this condition is not met, then the stall is sent in the next transaction. The CPU clears this bit after a host intervention.		
3	Tx Data Sequence(D0D1Sq) Software sets this bit and the hardware uses the corresponding DATA PID to transfer the FIFO data onto the bus.	0	Use Data 0 PID
		1	Use Data 1 PID
7:4	Byte Enables for the last Dword in the FIFO Software programs these bits to indicate the number of valid bytes in the last Dword in the FIFO. Software always does a 32-bit write to the FIFO	1111	All the bytes are valid in the last Dword
		0001	Only byte 1 is valid in the transfer. FIFOEMPTY-1[7:0] is the last byte of the transfer.
		0011	Only bytes 1 and 2 are valid in the transfer. FIFOEMPTY-1[15:0] are the last bytes of the transfer.
		0111	Only bytes 1, 2, and 3 are valid in the transfer. FIFOEMPTY-1[23:0] are the last bytes of the transfer.
8	Clear Tx FIFO Software writes to this bit to clear the transmission FIFO. The bit is cleared after the FIFO is cleared. Software should clear this bit.	0	Normal
		1	Clear the transmission FIFO

Register 4-111: End Point 0 Transmit Control Register (UD03R: Index 0Ch, Offset 100Ch)

Bit	Bit Definition	Bit Value	Value Definition
31:9	Reserved		

Register UD04R is the read status register for Transmit endpoint 0 (see *Register 4-112*). The lower byte of the register is updated on the rising edge of EOT. The value of this byte is valid only if EOT is a 1. The upper byte of the register has the transmit FIFO status and is updated whenever the transmit FIFO status changes. This is useful for a Poll mode of operation.

The lower byte of this register can be cleared by the software by writing a 1 to the corresponding bits.

Register 4-112: End Point 0 Transmit Status Register (UD04R: Index 10h, Offset 1010Ch)

Bit	Bit Definition	Bit Value	Value Definition
0	Acknowledge (ACK) This bit is set to 1 on the rising edge of the end of transaction (EOT) if the USB host receives an ACK.	0	Ack has not been received.
		1	Ack has been received.
1	Error (ERR) This bit is set to a 1 on the rising edge of EOT for any errors if NAK has not been asserted.	0	No Error.
		1	CRC error.
2	Time Out (TO) If there is a device time-out, this bit is set on the rising edge of the data packet EOT if NAK has not been asserted.	0	No Time Out.
		1	Timed Out.
3	End Of Transaction This bit is set on the rising edge of EOT of data packet.	0	No EOT.
		1	EOT.
5:4	Reserved		
6	Tx FIFO overrun Error This bit is set if the Tx FIFO has an overrun error during an IN transaction. When this happens the hardware asserts an EP0_tx_err signal. SIE will force a bit stuff error on the transmit packet.	0	No Error.
		1	Forced transmit Error.
7	Transaction NAKed This indicates that the hardware has issued a NAK. It is cleared by the software reading this bit.	0	Transaction not NAKed.
		1	NAKed transaction.
8	Reserved		
11:9	Tx FIFO Status Indicates the number of FIFO locations filled.	000	FIFO does not have any empty locations (FIFO is full).
		001	FIFO has one empty location.
		010	FIFO has two empty locations.
		011	FIFO has three empty locations.
		Others reserved	Reserved
31:12	Reserved	100	FIFO empty

Register UD05R is the read/write control register for Receive endpoint 0 (see *Register 4-113*).

Register 4-113: End Point 0 Receive Control Register (UD05R: Index 14h, 1014h)

Bit	Bit Definition	Bit Value	Value Definition
1:0	Reserved		
2	Send A Stall (SAS) This indicates that the function should send a STALL to the host. If this bit is asserted at least one clk12 cycle before the valid_token goes active for this transaction then the transaction is stalled. If this condition is not met, then the STALL is sent in the next transaction. This bit is cleared by the CPU after a host intervention.	0	Do not STALL transaction
		1	STALL the current transaction
7:3	Reserved		
8	Clear Rx FIFO CPU writes to this bit to clear the receiving FIFO. The bit is cleared after the FIFO is cleared.	0	Normal.
		1	Clear the receiving FIFO.
31:9	Reserved		

Register UD06R is the read status register for Receive endpoint 0. The lower byte of the register is updated on the rising edge of the EOT. The value of this byte is valid only if the EOT is a 1. The upper byte of the register has the receive FIFO status and is updated whenever the receive FIFO status changes. This is useful for a poll mode of operation.

The lower byte of this register can be cleared by the software by writing a 1 to the corresponding bits.

Register 4-114: End Point 0 Receive Status Register (UD06R: Index 18h, Offset 1018h)

Bit	Bit Definition	Bit Value	Value Definition
0	Acknowledge (ACK) This bit is set to 1 on the rising edge of EOT if an ACK is sent to the USB host.	0	ACK has not been sent.
		1	ACK has been sent.
1	Error (ERR) This bit is set to a 1 on the rising edge of the EOT for any CRC errors if NAK has not been asserted.	0	No Error.
		1	CRC error.
2	Time Out (TO) In case of a device time-out, this bit is set on the rising edge of the data packet EOT if NAK has not been asserted.	0	No Time Out.
		1	Timed Out.
3	End Of Transaction (EOT) This bit is set on the rising edge of the data packet EOT.	0	No EOT.
		1	EOT.
4	Rx Data Sequence Hardware sets this bit with the rising edge of the EOT if the transaction is not NAKed. Software reads this bit to correlate with data toggle sequence.	0	Data 0 PID.
		1	Data 1 PID.
5	Token Type This bit indicates whether the receive packet is a SETUP or OUT data packet.	0	OUT Packet.
		1	SETUP Packet.

Register 4-114: End Point 0 Receive Status Register (UD06R: Index 18h, Offset 1018h)

Bit	Bit Definition	Bit Value	Value Definition
6	Rx FIFO Overrun Error This bit is set if the receive FIFO has an over-run error during an OUT transaction. When this happens, the hardware asserts EP0_RX_ERR signal. SIE will not send an ACK.	0	No Error.
		1	Forced receive Error.
7	Transaction NAKed This indicates that a NAK has been issued by the hardware. It is cleared by the software reading this bit.	0	Transaction not NAKed.
		1	NAKed transaction
8	Reserved		
11:9	Rx FIFO Status Indicates the number of FIFO locations filled.	100	FIFO does not have any data items (FIFO is empty).
		011	FIFO has one data item.
		010	FIFO has two data items.
		001	FIFO has three data items.
		000	FIFO has four data items (FIFO is full).
13:12	Valid bytes in the Last Dword. Indicates the number of bytes valid in the last Dword in the FIFO.	00	All bytes are valid in the last Dword
		01	The lower byte [7:0] is valid in the last Dword
		10	The lower two bytes [15:0] are valid in the last Dword
		11	The lower three bytes [23:0] are valid in the last Dword
31:14	Reserved		

Register UD07R is a read-only register (see *Register 4-115*) and the endpoint 0 Rx FIFO register and the CPU accesses the endpoint 0 Rx FIFO through this register.

Register 4-115: End Point 0 Rx FIFO Register (UD07R: Index 1Ch, Offset 101Ch)

Bit	Bit Definition	Bit Value	Value Definition
31:0	Rx FIFO Data CPU reads these bytes.		

Register UD08R is a write-only register (see *Register 4-116*) and the endpoint 0 Tx FIFO register. CPU accesses the endpoint 0 Tx FIFO through this register.

Register 4-116: End Point 0 Tx FIFO Register (UD08R: Index 20h, Offset 1020h)

Bit	Bit Definition	Bit Value	Value Definition
31:0	Tx FIFO Data CPU writes these bytes.		

Register UD09R is the read/write control register for endpoint 1 (see *Register 4-117*). Endpoint 1 is the interrupt endpoint and is a Tx (IN transactions) only endpoint.

Register 4-117: End Point 1 Control Register (UD09R: Index 24h, Offset1024h)

Bit	Bit Definition	Bit Value	Value Definition
0	End Point Enable (EPE) This bit enables/disables the end point.	0	Disable the end point and clear the state machine and FIFO.
		1	Enable the end point.

Register 4-117: End Point 1 Control Register (UD09R: Index 24h, Offset1024h)

Bit	Bit Definition	Bit Value	Value Definition
1	End Of Data Transmit (EDT) This bit is valid only if the end point is configured as an IN. This indicates that the last byte of the data transmission is written into the FIFO. This bit is set by the CPU for CPU controlled writes, and is cleared by the hardware after the last byte is transmitted and ACKd.		
2	Send A STALL (SAS) This indicates that the function should send a STALL to the host. If this bit is asserted at least one clk12 cycle before the valid_token goes active for this transaction, then the transaction is Stalled. If this condition is not met, then the STALL is sent in the next transaction. This bit is cleared by the CPU after a host intervention. For EP0 this is always a 0.	0	Do not STALL transaction.
		1	STALL the current transaction.
3	Tx Data Sequence (D0D1Sq) The CPU sets this bit and the hardware uses the corresponding DATA PID to transfer the FIFO data onto the bus.	0	Use Data 0 PID.
		1	Use Data 1 PID.
7:4	Byte Enables for the last Dword in the FIFO These bits are programmed by software to indicate the number of valid bytes in the last Dword in the FIFO. Software always does a 32-bit write to the FIFO	1111	All the bytes are valid in the last Dword.
		0001	Only byte 1 is valid in the transfer. FIFOEMPTY-1[7:0] is the last byte of the transfer.
		0011	Only bytes 1 and 2 are valid in the transfer. FIFOEMPTY-1[15:0] are the last bytes of the transfer.
		0111	Only bytes 1, 2, and 3 are valid in the transfer. FIFOEMPTY-1[23:0] are the last bytes of the transfer.
8	Clear Tx FIFO CPU writes to this bit to clear the transmit FIFO. The bit is cleared after the FIFO is cleared. Software should clear this bit.	0	Normal.
		1	Clear the transmit FIFO.
31:9	Reserved		

Register UD0AR is the read status register for endpoint 1 (see *Register 4-118*). This register is updated on the rising edge of the EOT. The value of this register is valid only if the EOT is a 1. This is useful for a poll mode of operation. This is the transmission status register for EP1.

The lower byte of this register can be cleared by the software by writing a 1 to the corresponding bits.

Register 4-118: End Point 1 Status Register (UD0AR: Index 28h, Offset 1028h)

Bit	Bit Definition	Bit Value	Value Definition
0	Acknowledge (ACK) This bit is set to a 1 on the rising edge of the EOT if an ACK has been received from the USB host.	0	ACK has not been received.
		1	ACK has been received.
1	Error (ERR) This bit is set to a 1 on the rising edge of the EOT for any errors if NAK has not been asserted.	0	No Error.
		1	CRC error.

Register 4-118: End Point 1 Status Register (UD0AR: Index 28h, Offset 1028h)

Bit	Bit Definition	Bit Value	Value Definition
2	Time Out (TO) In case of a device time-out this bit is set on the rising edge of the EOT of the data packet if NAK has not been asserted.	0	No Time Out.
		1	Timed Out.
3	End Of Transaction (EOT) This bit is set on the rising edge of EOT of data packet.	0	No EOT.
		1	EOT.
5:4	Reserved		
6	Tx Error This bit is set if the transmit FIFO has an over-run error during an IN transaction. When this happens, the hardware asserts a EP1_tx_err signal. SIE forces a bit stuff error on the transmit packet.	0	No Error.
		1	Forced transmit Error.
7	Transaction NAKed This indicates that a NAK has been issued by the hardware. Software clears this bit.	0	Transaction not NAKed.
		1	NAKed transaction.
8	Reserved		
11:9	Tx FIFO Status Indicates the number of FIFO locations filled.	000	FIFO does not have any empty locations (FIFO is full).
		001	FIFO has one empty location.
		010	FIFO has two empty locations.
		011	FIFO has three empty locations.
		100	FIFO is empty.
31:12	Reserved		

Register UD0BR is a write-only register and the endpoint 1 transmit FIFO register (see *Register 4-119*). CPU accesses the endpoint 1 transmit FIFO through this register.

Register 4-119: End Point 1 Tx FIFO Register (UD0BR: Index 2Ch, Offset 102Ch)

Bit	Bit Definition	Bit Value	Value Definition
31:0	Tx FIFO Data CPU writes these bytes.		

Register UD0CR is the read/write control register for endpoint 2 (see *Register 4-120*). Endpoint 2 is the Bulk/ISO Tx end point (responds to in transactions only).

Register 4-120: End Point 2 Control Register (UD0CR: Index 30h, Offset 1030h)

Bit	Bit Definition	Bit Value	Value Definition
0	End Point Enable (EPE) This bit enables and disables the end point.	0	Disable the end point and clear the state machine and FIFO.
		1	Enable the end point.
1	Reserved		
2	Send A Stall (SAS) This indicates that the function should send a STALL to the host. If this bit is asserted at least one clk12 cycle before valid_token goes active, then the transaction is STALL. If this condition is not met, then the STALL is sent in the next transaction. The CPU clears this bit after a host intervention.	0	Do not STALL transaction.
		1	STALL the current transaction.
3	Tx Data Sequence(D0D1Sq) The CPU always initializes the DATA PID to DATA 0 PID at the beginning of a transfer. Subsequent packets use the data toggle synchronization and is done in hardware. The CPU write to this bit will override the DATA PID in use.	0	Don't change the PID.
		1	Use Data 0 PID for the next packet.
7:4	Reserved		
8	Clear Tx FIFO CPU writes to this bit to clear the transmit FIFO. The bit is cleared after the FIFO is cleared. Software should clear this bit.	0	Normal.
		1	Clear the transmit FIFO.
11:9	Tx FIFO Threshold Level – valid for ISOCHRONOUS transfers in DMA mode. The start address and the address latch are given along with the MIU request. The MIU continues incrementing the start address until the transaction size is complete. A new address with the address latch is given at the end of each transaction. A request is issued to the MIU every time the threshold drops with the burst length as the size. The burst length stays the same until the last request in a transaction. This sets the threshold level for the transmit FIFO. When the FIFO has the threshold number of empty locations, it makes a request to the MIU for a data fetch from the memory.	000	No request is generated.
		001	MIU request is generated whenever the FIFO has one location filled.
		010	MIU request is generated whenever the FIFO has two locations filled
		011	MIU request is generated whenever the FIFO has three locations filled
		100	MIU request is generated whenever the FIFO has four locations filled
		101	MIU request is generated whenever the FIFO has five locations filled
		110	MIU request is generated whenever the FIFO has six locations filled
		111	MIU request is generated whenever the FIFO has seven locations filled
31:12	Reserved		

Register UD0DR is a read-only register and the-read status register for endpoint 2 (see *Register 4-121*). This status is updated on a packet-by-packet basis.

Register 4-121: End Point 2 Status Register (UD0DR: Index 34h, Offset 1034h)

Bit	Bit Definition	Bit Value	Value Definition
0	Acknowledge (ACK) This bit is set to 1 on the rising edge of the EOT if an ACK has been received from the USB host.	0	ACK has not been received.
		1	ACK has been received.
1	Error (ERR) This bit is set to a 1 on the rising edge of the EOT for any CRC errors if NAK has not been asserted.	0	No Error.
		1	CRC error.
2	Time Out (TO) In case of a time out, this bit is set on the rising edge of the EOT of the data packet if NAK has not been asserted.	0	No Time Out.
		1	Timed Out.
3	End Of Transaction (EOT) This bit is set on the rising edge of the EOT of the data packet.	0	No EOT.
		1	EOT.
5:4	Reserved		
6	Tx Error This bit is set if the transmit FIFO has an over run error during an in transaction. When this happens, the hardware asserts the EP2_tx_err signal. SIE forces a bit stuff error on the transmit packet.	0	No Error.
		1	Forced transmit Error.
7	Transaction NAKed This indicates that a NAK has been issued by the hardware. Software clears this bit.	0	Transaction not And.
		1	NAKed transaction
31:8	Reserved		

Register UD0ER is the read/write control register for endpoint 3 (see *Register 4-122*). Endpoint 3 is the receive BULK/ISO endpoint (For OUT transactions).

Register 4-122: End Point 3 Control Register (UD0ER: Index 38h, Offset 1038h)

Bit	Bit Definition	Bit Value	Value Definition
0	End Point Enable (EPE) This bit enables and disables the end point.	0	Disable the end point and clear the state machine and FIFO.
		1	Enable the end point.
1	Reserved	0	No Error.
2	Send A Stall (SAS) This indicates that the function should send a STALL to the host. If this bit is asserted eight clk12 cycles after valid_token is asserted for this transaction, then the transaction is STALL. If this condition is not met, then the STALL is sent in the next transaction. The CPU clears this bit after a host intervention.	0	Do not STALL transaction
		1	STALL current transaction

Register 4-122: End Point 3 Control Register (UD0ER: Index 38h, Offset 1038h)

Bit	Bit Definition	Bit Value	Value Definition
3	Rx Data Sequence(D0D1Sq) The CPU always initializes the DATA PID to DATA 0 PID at the beginning of a transfer. Subsequent packets will use the data toggle synchronization and is done in hardware. In hardware we compare the incoming DATA PID and make a decision to drop or accept the current packet. The CPU write to this bit will override the DATA PID in use.	0	Don't change the PID.
		1	Use Data 0 PID for the next packet.
7:4	Reserved		
8	Clear Rx FIFO (CRF) CPU writes to this bit to clear the receive FIFO. The bit is reset after the FIFO is cleared. Software should clear this bit.	0	Normal.
		1	Clear the receive FIFO.
11:9	Rx FIFO Threshold Level – valid only for ISOCHRONOUS Transfers The start address for the first request is taken from the DMACR shadow register. The subsequent addresses are calculated at the end of each transaction. Each time a new address is presented to the MIU, an address latch is given. The address should be incremented by the MIU for all subsequent writes until a new address is received. In bulk mode the MIU request is generated after completely receiving the packet without any errors. The burst length is presented to the MIU along with the request. In isochronous mode the payload can be much larger than the FIFO size and more over there are no retries. Hence you can generate the request based on this threshold level. Each time the threshold is reached, a request to the MIU is generated along with the burst size. This sets the threshold level for the FIFO. When the receive FIFO has these many locations filled it makes a request to the MIU for a data read from FIFO. Legal Values are 1 to 11	000	No request or Interrupt is generated
		001	Request to MIU generated when FIFO has one location filled
		010	Request to MIU generated when FIFO has two locations filled
		011	Request to MIU generated when FIFO has three locations filled
		100	Request to MIU generated when FIFO has four locations filled
		101	Request to MIU generated when FIFO has five locations filled
		110	Request to MIU generated when FIFO has six locations filled
		111	Request to MIU generated when FIFO has seven locations filled
31:12	Reserved		

Register UD0FR is a read/writer register and the read status register for endpoint 3 (see *Register 4-123*). This register is updated on the rising edge of EOT. The value of this register is valid only if the EOT is a 1. This is the receive status register for EP3. This register is updated on a packet-by-packet basis.

Register 4-123: End Point 3 Status Register (UD0FR: Index 3Ch, Offset 103Ch)

Bit	Bit Definition	Bit Value	Value Definition
0	Acknowledge (ACK) This bit is set to a 1 on the rising edge of the EOT if an ACK is sent to the USB host for bulk transfers.	0	ACK has not been sent.
		1	ACK has been sent.
1	Error (ERR) This bit is set to a 1 on the rising edge of the EOT for any CRC errors if NAK has NOT been asserted.	0	No error.
		1	CRC error.
2	Time Out (TO) In case of a time-out this bit is set on the rising edge of the EOT of data packet if NAK has not been asserted.	0	No Time Out.
		1	Timed Out.
3	End Of Transaction (EOT) This bit is set on the rising edge of the EOT of data packet.	0	No EOT.
		1	EOT.
5:4	Reserved		
6	Rx Error This bit is set if the receive FIFO has an over-run error during an out transaction. When this happens, the hardware asserts the EP3_rx_err signal. SIE does not send an ACK for bulk transfers.	0	No error.
		1	Forced receive error.
7	Transaction NAKed This bit indicates that a NAK has been issued by the hardware. Software clears this bit.	0	Transaction not NAKed.
		1	NAKed transaction.
31:8	Reserved		

Register UD10R is a read/write register and the interrupt status register for the USB Device (see *Register 4-124*). This register is updated on the rising edge of EOT or SOF (if the respective interrupts are enabled). The value of this register is valid only if EOT is a 1. This register is updated on a packet-by-packet and frame basis.

Register 4-124: USB Device Interrupt Status Register (UD10R: Index 40h, Offset 1040h)

Bit	Bit Definition	Bit Value	Value Definition
0	SOF Interrupt This bit is set to a 1 by the hardware, on the rising edge of SOF token, if the SOF Interrupt is enabled (UD00R[16]). This bit is cleared when the software writes a 1 to this bit.	0	No Interrupt due to SOF.
		1	SOF Interrupt.
1	EP0 Transmit Interrupt This bit is set to a 1 by the hardware, on the rising edge of EOT, if the last packet was addressed from EP0-Tx and the EP0-Tx Interrupt is enabled (UD00R[17]). This bit is cleared when the software writes a 1 to this bit.	0	No Interrupt from EP0-Tx.
		1	Interrupt is from EP0-Tx.
2	EP0 Receive Interrupt This bit is set to a 1 by the hardware, on the rising edge of EOT, if the last packet was addressed to EP0-Rx and the EP0-Rx Interrupt is enabled (UD00R[18]). This bit is cleared when the software writes a 1 to this bit.	0	No Interrupt from EP0-Rx.
		1	Interrupt is from EP0-Rx.
3	EP1 Interrupt This bit is set to a ‘1’ by the hardware, on the rising edge of EOT, if the last packet was addressed from EP1 and the EP1 Interrupt is enabled (UD00R[19]). This bit is cleared when the software writes a “1” to this bit.	0	No Interrupt from EP1.
		1	Interrupt is from EP1.
4	EP2 Tx EOT Interrupt This bit is set to a ‘1’ by the hardware, on the rising edge of EOT, if the last packet was addressed from EP2 and the EP2 EOT Interrupt is enabled (UD00R[20]). This bit is cleared when the software writes a “1” to this bit.	0	No Interrupt from EP2.
		1	Interrupt is from EP2.
5	EP3 Rx EOT Interrupt This bit is set to a ‘1’ by the hardware, on the rising edge of EOT, if the last packet was addressed to EP3 and the EP3 Interrupt is enabled (UD00R[21]). This bit is cleared when the software writes a “1” to this bit.	0	Interrupt is not from EP3.
		1	Interrupt is from EP3.
6	Transmit buffer end hit interrupt for EP2 This bit is set to a ‘1’ by the hardware if the end of the current transmit buffer has been reached in the internal memory and the EP2 Interrupt is enabled (UD00R[22]). This bit is cleared when the software writes a “1” to this bit.	0	Interrupt is not from EP2.
		1	Interrupt is from EP2.

Register 4-124: USB Device Interrupt Status Register (UD10R: Index 40h, Offset 1040h)

Bit	Bit Definition	Bit Value	Value Definition
7	Receive buffer end hit interrupt for EP3 This bit is set to a "1" by the hardware if the end of the current receive buffer has been reached in the internal memory and the EP3 Interrupt is enabled (UD00R[23]). This bit is cleared when the software writes a "1" to this bit.	0	Interrupt is not from EP3.
		1	Interrupt is from EP3.
8	End of Receive transfer interrupt EP3 This bit is set to a "1" by the hardware if the end of receive transfer has, and the EP3 Interrupt is enabled (UD00R[24]). The end of transfer is detected when the device receives a zero length packet or a short packet (less than 64 bytes). This bit is cleared when the software writes a "1" to this bit.	0	Interrupt is not from EP3.
		1	Interrupt is from EP3.
9	Global suspend interrupt Host has put the device in suspend mode. Host stopped sending the SOFs for the last 5 frames. This interrupt is generated if UD00R[25] is "1".	0	Device is in normal operational mode.
		1	Device is in global suspend mode.
10	Wake up interrupt After the device is suspended potentially all the clocks will be stopped. In such a case if the USB Host sends resume signaling, this interrupt will be enabled if U00R[26] is "1". This can be used by the driver to start the clocks. Generation of this signal does not require a clock.	0	Resume signaling not detected
		1	Resume signaling detected
11	Reset signaling Interrupt This interrupt is generated if reset signaling is detected by the device during global suspend mode.	0	Reset signaling not detected
		1	Reset signaling detected
31:12	Reserved		

Register UD11R is a read/write, test control register (see *Register 4-125*). On reset this register comes up with a value 0000h. This register is used to load all counters in test mode, UD00R[24].

Register 4-125: USB Test Control Register (UD11R: Index 44h, Offset 1044h)

Bit	Bit Definition	Bit Value	Value Definition
0	Test Mode to read Counters used in Suspend, Wakeup logic. This bit if set will enable the three counters in the SWR block to count independently. This bit is also used to read the State machines from all the blocks. (Factory test mode only)	0	Test mode disable
		1	Test mode Enable
3:1	Test Mode to read the State machines directly. This bit if set can be used to read the state machines from all the blocks. The result will appear in the UD12R register. These bits are valid only if bit 0 is set. (Factory test mode only)	001	Use Main State Machine
		010	EP0 Rx State Machine
		011	EP0 Tx State Machine
		100	EP1 Tx State Machine
		101	EP2 Rx State Machine
		110	EP3 Tx State Machine
5:4	Counter select These bits select one of the three counters used in SUSPEND/WAKEUP logic. They are loaded with the value in the bits 14:8. (Factory test mode only)	00	Reserved
		01	Counter 1
		10	Counter 2
		11	Counter 3
7:6	Reserved		
14:8	Counter load value The counter selected by 1:0 will be loaded with this 7-bit value. (Factory test mode only)		
31:15	Reserved		

Register UD12R is a read only register (see *Register 4-126*). On reset this register comes up with a value 0000,0000h. Based on the test modes in the UD11R[1:0] the counter will be incremented by “1” and the result will be available in this register. This register should be read after one 12Mhz clock period.

Register 4-126: USB Test Control Register (UD12R: Index 48h, Offset 1048h)

Bit	Bit Definition	Bit Value	Value Definition
7:0	State Machine status In testmode the state machine of the selected test mode will be available in these bits.		
14:8	Counter result In testmode the selected counter will be loaded with the UD11R[14:8]. The counter will be incremented by “1” and the result will be available in these bits. (Factory test mode only)		
31:15	Reserved		

4.12.1. Suspend and Resume Logic

Whenever the USB line is idle for more than 3 milliseconds (ms) all devices enter into SUSPEND state. The device (or function) will exit the suspend state as soon as it sees any activity on the line. The HOST will send the resume signalling for 20ms and it will end the resume signalling with an EOP. If the device is capable of Remote wakeup it should wait for 5 ms before it signals resume signalling. It will signal for 11ms and then waits for resume signalling of 20ms from the HOST.

4.12.2. DMA Transfer and DMA Registers

To support large BULK and ISOCHRONOUS transfers we support the DMA mode of transfer to transfer data from CPU to the buffers in the internal SRAM. The CPU can first transfer the file to the internal buffer and then the data can be transferred from the MIU on a packet by packet basis. The following registers are used to support the DMA mode of transfer.

BULK Transfers

The DMA Controller can use either one buffer or two buffers for BULK transfers. In case of transmit the CPU can pre-fill the data in the buffer up to the buffer size and trigger the DMA Controller to transfer the first set of data to the End Point 2 FIFO. Every time an IN token is received the DMA controller will transmit the data in the buffer. Since the transfer size is known prior to transfer, the CPU provides the transfer size and the payload size for every IN token: 64 bytes (the packet size) is transferred.

At the end of Buffer-1, Buffer-2 is used if the second buffer is enabled. The DMA Controller will ping-pong between the two buffers. When a buffer is enabled and the “end of transfer” is enabled (UD18R[10]), a zero-length packet, or a short-packet, is sent when the buffer end is reached.

Single Transfers

In case of single transfer mode, the same buffer will be used continuously. At the end of the buffer, the current buffer pointer will point to the start of the buffer.

Isochronous Transfers

Since transmit data is continuous stream data, a continuous buffer can be used for Isochronous transfers. The DMA Controller will continuously fetch the data from the buffer. The packet size is the transfer size, and the address will be incremented by the DMA controller.

Bulk Receive

Every time the device receives the payload (64 bytes) it will request the MIU and transfer the data to the Buffer for BULK receive. Similar to transmit, either one buffer or two buffers can be used. Every time the buffer end is reached an interrupt will be generated to the CPU. Since the CPU has the start address it will empty the buffer. The last transfer can be less than the payload size. In this case the CPU will use the transfer size as described by the transfer registers (see *Register 4-133 on page 166* and *Register 4-134 on page 166*).

Isochronous Receive

A continuous buffer can be used for Isochronous receive. The DMA controller will constantly request the MIU to empty the data in the FIFO. Every time the buffer end is reached an interrupt is generated to the CPU. The CPU will empty the buffer depending on the size described by the transfer registers (see *Register 4-133 on page 166* and *Register 4-134 on page 166*).

Register 4-13 specifies the index and reset values for additional USB registers.

TABLE 4-13: Additional USB Register Index and Reset Values

Register	Index	Reset Value	Offset Value	See Description
UD18R	60h	0000-0000h	1060h	*Register 4-127 on page 162*
UD19R	64h	0000-0000h	1064h	*Register 4-128 on page 163*
UD1AR	68h	0000-0000h	1068h	*Register 4-129 on page 163*
UD1BR	6Ch	0000-0000h	106Ch	*Register 4-130 on page 164*
UD1CR	70h	0000-0000h	1070h	*Register 4-131 on page 165*
UD1DR	74h	0000-0000h	1074h	*Register 4-132 on page 165*
UD1ER	78h	0000-0000h	1078h	*Register 4-133 on page 166*
UD1FR	7Ch	0000-0000h	107Ch	*Register 4-134 on page 166*

Register UD18R is the read/write control register (see *Register 4-127*) for DMA transfers from system memory to internal buffers (EP2 endpoint).

Register 4-127: DMAC Control Register for CPU to Internal Buffer Transfers (UD18R: 60h, Offset 1060h)

Bit	Bit Definition	Bit Value	Value Definition
0	DMA Enable This bit enables/disables the DMA transfer from system memory to internal buffers.	0	Disable DMA
		1	Enable DMA
1	DMA Mode	0	Single Transfer In this mode at the end of the buffer, the buffer pointer will wrap around to the start of the buffer.
		1	Ping-Pong Buffer Mode At the end of Buffer-1, the DMA Controller will switch to Buffer-2.
3:2	Number of buffers used by the transmit path.	00	Single Buffer will be used
		01	2 buffers will be used. For ISO transfers, this selection should be used.
		10	Reserved
		11	Reserved
7:4	Reserved		
8	EP2 Buffer-1 owner	0	Software/CPU is the owner of the buffer. To start with CPU owns the buffer. Once it fills up it can set it to “1” to let Device own the buffer.
		1	USB Device is the owner. After reaching the end of the buffer, Device will interrupt the CPU and clear this bit.
9	EP2 Buffer-2 owner	0	Software/CPU is the owner of the buffer. To start with CPU owns the buffer. Once it fills up it can set it to “1” to let Device own the buffer.
		1	USB Device is the owner. After reaching the end of the buffer, Device will interrupt the CPU and clear this bit.
10	Send end of transfer with Buffer-1. Valid only in BULK mode.	0	End of the transfer has not yet reached with this buffer.
		1	The transfer ends when the Buffer-1 end is reached. Device will either send a short-packet or a zero-length packet to USB Host.
11	Send end of transfer with Buffer-2. Valid only in BULK mode.	0	End of the transfer has not yet reached with this buffer.
		1	The transfer ends when the Buffer-2 end is reached. Device will either send a short-packet or a zero-length packet to USB Host.
31:12	Reserved		

Register UD19R is the read/write size/address register for DMA transfers from system memory to internal buffers (see *Register 4-128*). This register is used to program the Start Address of Buffer-1 and the Buffer size.

Register 4-128: Buffer-1 Start Address and Size for Writes from System Memory to Internal Buffers (UD19R: Index 64h, Offset 1064h)

Bit	Bit Definition	Bit Value	Value Definition
14:0	Buffer-1 Start Address These bits define the 64-bit start address for Buffer-1. This forces the buffer address to be at 64-bit boundary.		
15	Reserved		
27:16	Buffer-1 Size The actual buffer size is programmed here. This value gives the buffer size in bytes - 1. The maximum buffer size allowed is 4 Kbyte. In case of bulk transfers, this has to be multiples of 64 bytes except for the last buffer of transmit. For ISO transfers, buffer size should be equal to packet size.		
28	Last buffer enable	0	Indicating that Buffer-1 is not the last buffer of the transfer or does not contain exact multiples of 64 bytes.
		1	Indicating that Buffer-1 contains the last set of exact multiples of 64 bytes to be transferred.
31-29	Reserved		

Register UD1AR is the read/write size/address register for DMA transfers from system memory to the internal buffers (see *Register 4-129*). This register is used to program the Start Address of Buffer-2 and the buffer size.

Register 4-129: Buffer-2 Start Address and Size for Writes from System Memory to Internal Buffers (UD1AR: Index 68h, Offset 1068h)

Bit	Bit Definition	Bit Value	Value Definition
14:0	Buffer-2 Start Address These bits define the 64-bit start address for Buffer-2. This forces the buffer address to be at 64-bit boundary.		
15	Reserved		
27:16	Buffer-2 Size The actual buffer size is programmed here. This value gives the buffer size in bytes - 1. The maximum buffer size allowed is 4 Kbytes. In case of bulk transfers, this has to be multiples of 64 bytes except for the last buffer of transmit. For ISO transfers, buffer size should be equal to packet size.		
28	Last buffer enable	0	Indicating that Buffer-2 is not the last buffer of the transfer, or does not contain exact multiples of 64 bytes.
		1	Indicating that Buffer-2 contains the last set of exact multiples of 64 bytes to be transferred.
31-29	Reserved		

Register UD1BR is the read/write control register (see *Register 4-130*) for DMA transfers from internal buffer to system memory (EP3 endpoint).

Register 4-130: DMAC Control Register for Internal Buffers to System Memory Transfers (UD1BR: Index 6Ch, Offset 106Ch)

Bit	Bit Definition	Bit Value	Value Definition
0	DMA Enable This bit enables/disables the DMA transfer from internal memory to system memory.	0	Disable DMA
		1	Enable DMA
1	DMA Mode	0	Single Transfer In this mode at the end of the buffer, the buffer pointer will wrap around to the start of the buffer.
		1	Ping-Pong buffer Mode At the end of Buffer-1, the DMA Controller will switch to Buffer-2.
3:2	Number of buffers used by the receive path.	00	Single buffer will be used
		01	2 buffers will be used.
		10	Reserved
		11	Reserved
7:4	Reserved		
8	EP3 Buffer-1 owner	0	Device is the owner of the buffer. To start with Device owns the buffer. Once it fills up it can set it to “1” to let software/CPU own the buffer. Device will interrupt the CPU.
		1	Software/CPU is the owner. After emptying the buffer, software will clear this bit.
9	EP3 Buffer-2 owner	0	Device is the owner of the buffer. To start with Device owns the buffer. Once it fills up it can set it to “1” to let software/CPU own the buffer. Device will interrupt the CPU.
		1	Software/CPU is the owner. After emptying the buffer, software will clear this bit.
10	End of transfer or buffer received with Buffer-1. This bit is set by the device. It is valid only in BULK modes. The software should pick the transfer size of the buffer from the Receive size register (UD1FR).	0	End of the transfer has not yet reached with this buffer.
		1	The transfer ends when the Buffer-1 end is reached. USB Host device either sent a short-packet or a zero-length packet to device.
11	End of transfer or buffer received with Buffer-2. This bit is set by the device. It is valid only in BULK transfer mode. The software should pick the transfer size of the buffer from the Receive size register (UD1ER).	0	End of the transfer or buffer has not yet reached with this buffer.
		1	The transfer or buffer ends when the Buffer-2 end is reached. USB Host either sent a short-packet or a zero-length packet to device.
15:12	Reserved		
16	ISO receive transfer end command bit.	0	End of the transfer has not yet reached.
		1	Terminates ISO receive transfer.
31:17	Reserved		

Register UD1CR is the read/write, start/end register for DMA transfers from internal buffers to system memory. This register is used to program the Start Address of Buffer-1 and the buffer size (see *Register 4-131*).

Register 4-131: Buffer-1 Start Address and Size for Writes from Internal Buffers to System Memory (UD1CR: Index 70h, Offset 1070h)

Bit	Bit Definition	Bit Value	Value Definition
14:0	Buffer-1 Start Address These bits define the start address for the Buffer-1 and is restricted to the 64-bit boundary.		
15	Reserved		
30:16	Buffer-1 End Address These bits define the end address for the Buffer-1 and is restricted to the 64-bit boundary. Buffer size should be multiples of 64 bytes in case of bulk mode receive.		
31	Reserved		

Register UD1DR is the read/write, start/end register, for DMA transfers from internal buffers to system memory (see *Register 4-132*). This register is used to program the Start Address of Buffer-2 and the buffer size.

Register 4-132: Buffer-2 Start Address and Size for Writes from Internal Buffers to System Memory (UD1DR: Index 74h, Offset 1074h)

Bit	Bit Definition	Bit Value	Value Definition
14:0	Buffer-2 Start Address These bits define the start address for the Buffer-2 and is restricted to the 64-bit boundary.		
15	Reserved		
30:16	Buffer-2 End Address These bits define the end address for the Buffer-2 and is restricted to the 64-bit boundary. Buffer size should be multiples of 64 bytes in case of bulk mode receive.		

Register UD1ER is the read/write transfer size register for the last DMA transfers from internal buffers to system memory if the end-of-transfer is reached in Buffer-1 (see *Register 4-133*). The DMA controller writes the transfer size of the data in the last buffer to this register. CPU/Software should use this only when the corresponding "end-of-transfer" reached (UD1BR[10]) is set.

Register 4-133: Transfer Size Register if the End-of-Transfer is Reached in Buffer-1 (UD1ER: Index 78h, Offset 1078h)

Bit	Bit Definition	Bit Value	Value Definition
12:0	Transfer size of the last buffer's receive data. These bits define the amount of valid data in the Buffer-1 and is valid only if the UD1BR[10] is set. If the transfer size spawns multiple buffers, each time a buffer end is reached the DMA controller will switch to the next buffer. This will go on until the last buffer. The last buffer might not have the buffer size amount of valid data. This register will give the amount of valid data in the buffer.		
15:13	Reserved		
31:16	Reserved		

Register UD1FR is the read/write Transfer size register for the last DMA transfers from internal buffers to system memory if the end-of-transfer is reached in Buffer-2 (see *Register 4-134*). The DMA controller writes the transfer size of the data in the last buffer to this register. CPU/Software should use this only when the corresponding "end-of-transfer" reached (UD1BR[11]) is set.

Register 4-134: Transfer Size Register if the End-of-Transfer is Reached in Buffer-2 (UD1FR: Index 7Ch, Offset 107Ch)

Bit	Bit Definition	Bit Value	Value Definition
12:0	Transfer size of the last buffer's receive data. These bits define the amount of valid data in the Buffer-2 and is valid only if the UD1BR[11] is set. If the transfer size spawns multiple buffers, each time a buffer end is reached the DMA controller will switch to the next buffer. This will go on until the last buffer. The last buffer might not have the buffer size amount of valid data. This register will give the amount of valid data in the buffer.		
15:13	Reserved		
31:16	Reserved		

4.13 USB Host Module (MQ-1132 only)

The MQ-1132 USB is a low to mid-speed serial communications bus that operates at 12 Mbps, with a 1.5 Mbps sub-channel for cost-sensitive applications. USB is a master/slave type of bus. There is a USB host that is responsible for scheduling the bus and various devices that can be either hubs or functions that share the serial data stream. The actual topology of the bus is best described as a tiered star network.

All devices are connected over a four wire cable, no longer than 5 meters. Two of the wires are a twisted pair carrying differential data, while the other pair of wires provides a limited amount of power so that the devices may be powered off the bus itself. Data is transferred using Non-return to zero inverted (NRZI) encoding at 12 Mbps. There is also a 1.5 Mbps sub-channel that can be simultaneously supported on the same wires. Each functional device must plug into a special type of USB device called hub.

Hubs are intelligent devices that not only act as signal repeaters and routers, but also provide some basic power management. Hubs are essential to the plug and play implementation. Each hub has the ability to control the power applied to devices connected downstream from it, as well as notifying the host when a device has been connected or disconnected from the network. Once a device is connected to the network and completes the enumeration process, the hubs act as repeaters and become transparent from the data flow perspective.

The USB hoist interface to the computer system is the host controller. A root hub is integrated within the host system to provide the attachment points or port.

There is one register set in the MQ-1132 USB host controller module: OHCI register.

4.13.1. OHCI Registers

The following section defines the OHCI Registers within the Host Controller.

The Host Controller (HC) contains a set of on-chip operational registers which are mapped into a noncacheable portion of the system addressable space. These registers are used by the Host Controller Driver (HCD). According to the function of these registers, they are divided into four partitions, specifically for Control and Status, Memory Pointer, Frame Counter and Root Hub. All of the registers will be read and written as Dwords.

Reserved bits may be allocated in future releases of this specification. To ensure interoperability, the Host Controller Driver that does not use a reserved field should not assume that the reserved field contains 0. Furthermore, the Host Controller Driver should always preserve the value(s) of the reserved field. When a R/W register is modified, the Host Controller Driver should first read the register, modify the bits desired, then write the register with the reserved bits still containing the read value. Alternatively, the Host Controller Driver can maintain an in-memory copy of previously written values that can be modified and then written to the Host Controller register. When a write to set/clear register is written, bits written to reserved fields should be 0.

Table 4-14 includes the index, offset, and reset values for the host controller operation registers.

TABLE 4-14: Host Controller Operation Register Index and Reset Values

Register	Index	Offset	Reset Value	See Description
OH00R	00h	500h	xxxx-xx10h	*Register 4-135 on page 168*
OH01R	04h	504h	0000-0000h	*Register 4-136 on page 169*
OH02R	08h	508h	0000-0000h	*Register 4-137 on page 171*
OH03R	0Ch	50Ch	0000-0000h	*Register 4-138 on page 173*
OH04R	10h	510h	0000-0000h	*Register 4-139 on page 174*
OH05R	14h	514h	0000-0000h	*Register 4-140 on page 175*
OH06R	18h	518h	0000-0000h	*Register 4-141 on page 175*
OH07R	1Ch	51Ch	0000-0000h	*Register 4-142 on page 176*
OH08R	20h	520h	0000-0000h	*Register 4-143 on page 176*
OH09R	24h	524h	0000-0000h	*Register 4-144 on page 176*
OH0AR	28h	528h	0000-0000h	*Register 4-145 on page 177*
OH0BR	2Ch	52Ch	0000-0000h	*Register 4-146 on page 177*
OH0CR	30h	530h	0000-0000h	*Register 4-147 on page 177*
OH0DR	34h	534h	0000-2edfh	*Register 4-148 on page 178*
OH0ER	38h	538h	0000-0000h	*Register 4-149 on page 178*
OH0FR	3Ch	53Ch	0000-0000h	*Register 4-150 on page 179*
OH10R	40h	540h	xxxx-0000h	*Register 4-151 on page 179*
OH11R	44h	544h	0000-0628h	*Register 4-152 on page 179*
OH12R	48h	548h	0000-1102h	*Register 4-153 on page 180*
OH13R	4Ch	54Ch	0000-0000h	*Register 4-154 on page 181*
OH14R	50h	550h	0000-0000h	*Register 4-155 on page 182*
OH15R	54h	554h	0000-0000h	*Register 4-156 on page 183*
OH16R	58h	558h	0000-0000h	*Register 4-157 on page 187*

Register UH00R, a read-only register, has the host controller's revision ID (see *Register 4-135*).

Register 4-135: HcRevision Register (UH00R: Index 00h, Offset 500h)

Bit	Bit Definition	Bit Value	Value Definition
7:0	Revision This read-only field contains the BCD representation of the version of the HCI specification that is implemented by this HC. For example, a value of 11h corresponds to version 1.1. All of the HC implementations that are compliant with this specification will have a value of 10h.		
31:8	Reserved		

The HcControl register, a read/write register, defines the operating modes for the Host Controller (see *Register 4-136*). Most of the fields in this register are only modified by the Host Controller Driver, except Host Controller Functional State and Remote Wakeup Connected.

Register 4-136: HcControl Register (UH01R: Index 04h, Offset 504h)

Bit	Bit Definition	Bit Value	Value Definition
1:0	Control Bulk Service Ratio This specifies the service ratio between Control and Bulk EDs. Before processing any of the nonperiodic lists, HC must compare the ratio specified with its internal count on how many non-empty Control EDs have been processed, in determining whether to continue serving another Control ED or switching to Bulk EDs. The internal count will be retained when crossing the frame boundary. In case of reset, HCD is responsible for restoring this value.	00	One Control ED is served every time one Bulk ED is served.
		01	Two Control EDs are served every time one Bulk ED is served.
		10	Three Control EDs are served every time one Bulk ED is served.
		11	Four Control EDs are served every time one Bulk ED is served.
2	Periodic List Enable This bit is set to enable the processing of the periodic list in the next frame. If cleared by the HCD, processing of the periodic list does not occur after the next SOF. HC must check this bit before it starts processing the list.		
3	Isochronous Enable This bit is used by HCD to enable/disable processing of isochronous EDs. While processing the periodic list in a Frame, HC checks the status of this bit when it finds an Isochronous ED (F=1). If set (enabled), HC continues processing the EDs. If cleared (disabled), HC halts processing of the periodic list (which now contains only isochronous EDs) and begins processing the Bulk/Control lists. Setting this bit is guaranteed to take effect in the next Frame (not the current Frame).		
4	Control List Enable This bit is set to enable the processing of the Control list in the next Frame. If cleared by HCD, processing of the Control list does not occur after the next SOF. HC must check this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcControlCurrentED is pointing to an ED to be removed, HCD must advance the pointer by updating HcControlCurrentED before re-enabling processing of the list.		

Register 4-136: HcControl Register (UH01R: Index 04h, Offset 504h)

Bit	Bit Definition	Bit Value	Value Definition
5	Bulk List Enable This bit is set to enable the processing of the Bulk list in the next Frame. If cleared by HCD, processing of the Bulk list does not occur after the next SOF. HC checks this bit whenever it determines to process the list. When disabled, HCD may modify the list. If *HcBulkCurrentED* is pointing to an ED to be removed, HCD must advance the pointer by updating *HcBulkCurrentED* before re-enabling processing of the list.		
7:6	Host Controller Functional State A transition to USBOPERATIONAL from another state causes SOF generation to begin 1 ms later. HCD may determine whether HC has begun sending SOFs by reading the **Start of Frame** field of *HcInterruptStatus*. This field may be changed by HC only when in the USBSUSPEND state. HC may move from the USBSUSPEND state to the USBRESUME state after detecting the resume signaling from a downstream port. HC enters USBSUSPEND after a software reset, whereas it enters USBRESET after a hardware reset. The latter also resets the Root Hub and asserts subsequent reset signaling to downstream ports.	00	USB Reset
		01	USB Resume
		10	USB Operational
		11	USB Suspend
8	Interrupt Routing This bit determines the routing of interrupts generated by events registered in *HcInterruptStatus*. If clear, all interrupts are routed to the normal host bus interrupt mechanism. If set, interrupts are routed to the System Management Interrupt. HCD clears this bit upon a hardware reset, but it does not alter this bit upon a software reset. HCD uses this bit as a tag to indicate the ownership of HC.		
9	Remote Wakeup Connected This bit indicates whether HC supports remote wakeup signaling. Since we support Remote Wakeup it is the responsibility of system firmware to set this bit during enumeration. HC clears the bit upon a hardware reset but does not alter it upon a software reset.		

Register 4-136: HcControl Register (UH01R: Index 04h, Offset 504h)

Bit	Bit Definition	Bit Value	Value Definition
10	Remote Wakeup Enable This bit is used by HCD to enable or disable the remote wakeup feature upon the detection of upstream resume signaling. When this bit is set and the **Resume Detected** bit in *HcInterruptStatus* is set, a remote wakeup is signaled to the host system. Setting this bit has no impact on the generation of hardware interrupt.		
31:11	Reserved		

The HcCommandStatus register (see *Register 4-137*) is used by the Host Controller to receive commands issued by the Host Controller Driver, as well as reflecting the current status of the Host Controller. To the Host Controller Driver, it appears to be a 'write to set' register. The Host Controller will ensure that bits written as '1' become set in the register while bits written as '0' remain unchanged in the register. The Host Controller Driver may issue multiple distinct commands to the Host Controller without concern for corrupting previously issued commands. The Host Controller Driver has normal read access to all bits.

The Scheduling Overrun Count field indicates the number of frames with which the Host Controller has detected the scheduling overrun error. This occurs when the Periodic list does not complete before EOF. When a scheduling overrun error is detected, the Host Controller increments the counter and sets the Scheduling Overrun field in the HcInterruptStatus register.

Register 4-137: HcCommandStatus Register (UH02R: Index 08h, Offset 508h)

Bit	Bit Definition	Bit Value	Value Definition
0	Host Controller Reset (R/W) This bit is set by HCD to initiate a software reset of HC. Regardless of the functional state of HC, it moves to the UsbSuspend state in which most of the operational registers are reset except those stated otherwise; e.g., the Interrupt Routing field of HcControl, and no Host bus accesses are allowed. This bit is cleared by HC upon the completion of the reset operation. The reset operation must be completed within 10 ms. This bit, when set, should not cause a reset to the Root Hub and no subsequent reset signaling should be asserted to its downstream ports.		

Register 4-137: HcCommandStatus Register (UH02R: Index 08h, Offset 508h)

Bit	Bit Definition	Bit Value	Value Definition
1	Control List Filled (R/W) This bit is used to indicate whether there are any TDs on the Control list. It is set by HCD whenever it adds a TD to an ED in the Control list. When HC begins to process the head of the Control list, it checks CLF. As long as Control List Filled is 0, HC will not start processing the Control list. If CF is 1, HC will start processing the Control list and will set Control List Filled to 0. If HC finds a TD on the list, then HC will set Control List Filled to 1 causing the Control list processing to continue. If no TD is found on the Control list, and if the HCD does not set Control List Filled, then Control List Filled will still be 0 when HC completes processing the Control list and Control list processing will stop.		
2	Bulk List Filled (R/W) This bit is used to indicate whether there are any TDs on the Bulk list. It is set by HCD whenever it adds a TD to an ED in the Bulk list. When HC begins to process the head of the Bulk list, it checks BF. As long as Bulk List Filled is 0, HC will not start processing the Bulk list. If Bulk List Filled is 1, HC will start processing the Bulk list and will set BF to 0. If HC finds a TD on the list, then HC will set Bulk List Filled to 1 causing the Bulk list processing to continue. If no TD is found on the Bulk list, and if HCD does not set Bulk List Filled, then Bulk List Filled will still be 0 when HC completes processing the Bulk list and Bulk list processing will stop.		
3	Ownership Change Request (R/W) This bit is set by an OS HCD to request a change of control of the HC. When set HC will set the Ownership Change field in HcInterruptStatus. After the change over, this bit is cleared and remains so until the next request from OS HCD.		
15:4	Reserved		
17:16	Scheduling Overrun Count (R) These bits are incremented on each scheduling overrun error. It is initialized to 00b and wraps around at 11b. This will be incremented when a scheduling overrun is detected even if **Scheduling Overrun** in *HcInterruptStatus* has already been set. This is used by HCD to monitor any persistent scheduling problems.		
31-18	Reserved		

The HcInterruptStatus register, a read/write register, provides status on various events that cause hardware interrupts (see *Register 4-138*). When an event occurs, HC sets the corresponding bit in this register. When a bit becomes set, a hardware interrupt is generated if the interrupt is enabled in the HcInterruptEnable register and the Master Interrupt Enable bit is set. The Host Controller Driver may clear specific bits in this register by writing '1' to bit positions to be cleared. The Host Controller Driver may not set any of these bits. The HC will never clear the bit.

Register 4-138: HcInterruptStatus Register (UH03R: Index 0Ch, Offset 50Ch)

Bit	Bit Definition	Bit Value	Value Definition
0	Scheduling Overrun This bit is set when the USB schedule for the current Frame overruns and after the update of HccaFrameNumber. A scheduling overrun will also cause the Scheduling Overrun Count of *HcCommandStatus* to be incremented.		
1	Writeback Done Head This bit is set immediately after HC has written HcDoneHead to HccaDoneHead. Further updates of the HccaDoneHead will not occur until this bit has been cleared. HCD should only clear this bit after it has saved the content of HccaDoneHead.		
2	Start of Frame This bit is set by HC at each start of a frame and after the update of HccaFrameNumber. HC also generates a SOF token at the same time.		
3	Resume Detected This bit is set when HC detects that a device on the USB is asserting resume signaling. It is the transition from no resume signaling to resume signaling causing this bit to be set. This bit is not set when HCD sets the USBRESUME state.		
4	Unrecoverable Error This bit is set when HC detects a system error not related to USB. HC should not proceed with any processing or signaling before the system error has been corrected. HCD clears this bit after HC has been reset.		
5	Frame Number Overflow This bit is set when the MSb of HcFmNumber (bit 15) changes value, from '0' to '1' or from '1' to '0', and after HccaFrameNumber has been updated.		
6	Root Hub Status Change This bit is set when the content of HcRhStatus or the content of any of HcRhPortStatus1 or HcRhPortStatus2 has changed.		
29:7	Reserved		

Register 4-138: HcInterruptStatus Register (UH03R: Index 0Ch, Offset 50Ch)

Bit	Bit Definition	Bit Value	Value Definition
30	Ownership Change This bit is set by HC when HCD sets the **Ownership Change** Request field in *HcCommandStatus*. This event, when unmasked, will always generate an System Management Interrupt (SMI) immediately. This bit is tied to '0' when the SMI pin is not implemented.		
31	Reserved		

Each enable bit in the HcInterruptEnable register, a read/write register (see *Register 4-139*), corresponds to an associated interrupt bit in the HcInterruptStatus register. The HcInterruptEnable register is used to control which events generate a hardware interrupt. When a bit is set in the HcInterruptStatus register and the corresponding bit in the HcInterruptEnable register is set and the Master Interrupt Enable bit is set, then a hardware interrupt is requested on the host bus.

Writing a '1' to a bit in this register sets the corresponding bit, whereas writing a '0' to a bit in this register leaves the corresponding bit unchanged. On read, the current value of this register is returned.

Register 4-139: HcInterruptEnable Register (UH04R: Index 10h, Offset 510h)

Bit	Bit Definition	Bit Value	Value Definition
0	Scheduling Overrun	0	Ignore this bit.
		1	Enable Interrupt generation due to scheduling Overrun.
1	Writeback Done Head	0	Ignore this bit.
		1	Enable Interrupt generation due to HcDoneHead Write back.
2	Start of Frame	0	Ignore this bit.
		1	Enable Interrupt generation due to Start of Frame.
3	Resume Detect	0	Ignore this bit.
		1	Enable Interrupt generation due to Resume Detect.
4	Unrecoverable Error	0	Ignore this bit.
		1	Enable Interrupt generation due to Unrecoverable Error.
5	Frame Number Overflow	0	Ignore this bit.
		1	Enable Interrupt generation due to Frame Number Overflow.
6	Root Hub Status Change	0	Ignore this bit.
		1	Enable Interrupt generation due to Root Hub Status Change.
29:7	Reserved		
30	Ownership Change	0	Ignore this bit.
		1	Enable Interrupt generation due to Ownership Change.
31	Master Interrupt Enable A '0' written to this field is ignored by HC. A '1' written to this field enables interrupt generation due to events specified in the other bits of this register. This is used by HCD as a Master Interrupt Enable.		

Each disable bit in the HcInterrupt Enable register, a read/write register (see *Register 4-140*) corresponds to an associated interrupt bit in the HcInterruptStatus register. The HcInterruptDisable register is coupled with the HcInterruptEnable register. Thus, writing a '1' to a bit in this register clears the corresponding bit in the HcInterruptEnable register, whereas writing a '0' to a bit in this register leaves the corresponding bit in the HcInterruptEnable register unchanged. On read, the current value of the HcInterruptEnable register is returned.

Register 4-140: HcInterruptDisable Register (UH05R: Index 14h, Offset 514h)

Bit	Bit Definition	Bit Value	Value Definition
0	Scheduling Overrun	0	Ignore this bit.
		1	Disable Interrupt generation due to scheduling Overrun.
1	Writeback Done Head	0	Ignore this bit.
		1	Disable Interrupt generation due to HcDoneHead Write back.
2	Start of Frame	0	Ignore this bit.
		1	Disable Interrupt generation due to Start of Frame.
3	Resume Detect	0	Ignore this bit.
		1	Disable Interrupt generation due to Resume Detect.
4	Unrecoverable Error	0	Ignore this bit.
		1	Disable Interrupt generation due to Unrecoverable Error.
5	Frame Number Overflow	0	Ignore this bit.
		1	Disable Interrupt generation due to Frame Number Overflow.
6	Root Hub Status Change	0	Ignore this bit.
		1	Disable Interrupt generation due to Root Hub Status Change.
29:7	Reserved		
30	Ownership Change	0	Ignore this bit.
		1	Disable Interrupt generation due to Ownership Change.
31	Master Interrupt Enable A '0' written to this field is ignored by HC. A '1' written to this field enables interrupt generation due to events specified in the other bits of this register. This is used by HCD as a Master Interrupt Enable.		

The HcHCCA register, a read/write register (see *Register 4-141*) contains the physical address of the Host Controller Communication Area. The Host Controller Driver determines the alignment restrictions by writing all 1s to HcHCCA and reading the content of HcHCCA. The alignment is evaluated by examining the number of zeroes in the lower order bits. The minimum alignment is 256 bytes; therefore, bits 0 through 7 must always return '0' when read. This area is used to hold the control structures and the Interrupt table that are accessed by both the Host Controller and the Host Controller Driver.

Register 4-141: HcHCCA Register (UH06R: Index 18h, Offset 518h)

Bit	Bit Definition	Bit Value	Value Definition
7:0	Reserved		
31:8	HCCA This is the base address of the Host Controller Communication Area.		

The HcPeriodCurrentED register, read-only register (see *Register 4-142*), contains the physical address of the current Isochronous or Interrupt Endpoint Descriptor.

Register 4-142: HcPeriodCurrentED Register (UH07R: Index 1Ch, Offset 51Ch)

Bit	Bit Definition	Bit Value	Value Definition
3:0	Reserved		
31:4	Periodic Current ED This is used by HC to point to the head of one of the Periodic lists which will be processed in the current Frame. The content of this register is updated by HC after a periodic ED has been processed. HCD may read the content in determining which ED is currently being processed at the time of reading.		

The HcControlHeadED register, a read/write register (see *Register 4-143*) contains the physical address of the first Endpoint Descriptor of the Control list.

Register 4-143: HcPeriodCurrentED Register (UH08R: Index 20h, Offset 520h)

Bit	Bit Definition	Bit Value	Value Definition
3:0	Reserved		
31:4	Control Head ED HC traverses the Control list starting with the *HcControlHeadED* pointer. The content is loaded from HCCA during the initialization of HC.		

The HcControlCurrentED register, a read/write register (see *Register 4-144*) contains the physical address of the current Endpoint Descriptor of the Control list.

Register 4-144: HcControlCurrentED Register (UH09R: Index 24h, Offset 524h)

Bit	Bit Definition	Bit Value	Value Definition
3:0	Reserved		
31:4	Control Current ED This pointer is advanced to the next ED after serving the present one. HC will continue processing the list from where it left off in the last Frame. When it reaches the end of the Control list, HC checks the **Control List Filled** of in *HcCommandStatus*. If set, it copies the content of *HcControlHeadED* to *HcControlCurrentED* and clears the bit. If not set, it does nothing. HCD is allowed to modify this register only when the **Control List Enable** of *HcControl* is cleared. When set, HCD only reads the instantaneous value of this register. Initially, this is set to zero to indicate the end of the Control list.		

The HcBulkHeadED register, a read/write register (see *Register 4-145*), contains the physical address of the first Endpoint Descriptor of the Bulk list.

Register 4-145: HcBulkHeadED Register (UH0AR: Index 28h, Offset 528h)

Bit	Bit Definition	Bit Value	Value Definition
3:0	Reserved		
31:4	Bulk Head ED HC traverses the Bulk list starting with the HcBulkHeadED pointer. The content is loaded from HCCA during the initialization of HC.		

The HcBulkCurrentED register, a read/write register (see *Register 4-146*), contains the physical address of the current endpoint of the Bulk list. As the Bulk list will be served in a round-robin fashion, the end points will be ordered according to their insertion to the list.

Register 4-146: HcBulkCurrentED Register (UH0BR: Index 2Ch, Offset 52Ch)

Bit	Bit Definition	Bit Value	Value Definition
3:0	Reserved		
31:4	Bulk Current ED This is advanced to the next ED after the HC has served the present one. HC continues processing the list from where it left off in the last Frame. When it reaches the end of the Bulk list, HC checks the **Control List Filled** of HcControl. If set, it copies the content of *HcBulkHeadED* to *HcBulkCurrentED* and clears the bit. If it is not set, it does nothing. HCD is only allowed to modify this register when the **Bulk List Enable** of *HcControl* is cleared. When set, the HCD only reads the instantaneous value of this register. This is initially set to zero to indicate the end of the Bulk list.		

The HcDoneHead register, a read-only register (see *Register 4-147*), contains the physical address of the last completed Transfer Descriptor that was added to the Done queue. In normal operation, the Host Controller Driver should not need to read this register as its content is periodically written to the HCCA.

Register 4-147: HcDoneHead Register (UH0CR: Index 30h, Offset 530h)

Bit	Bit Definition	Bit Value	Value Definition
3:0	Reserved		
31:4	Done Head When a TD is completed, HC writes the content of HcDoneHead to the NextTD field of the TD. HC then overwrites the content of HcDoneHead with the address of this TD. This is set to zero whenever HC writes the content of this register to HCCA. It also sets the Writeback Done Head of HcInterruptStatus.		

The HcFmInterval register, a read/write register (see *Register 4-148*), contains a 14-bit value which indicates the bit time interval in a Frame, (for example: between two consecutive SOFs), and a 15-bit value indicating the Full Speed maximum packet size that the Host Controller may transmit or receive without causing scheduling overrun. The Host Controller Driver may carry out minor adjustment on the Frame Interval by writing a new value over the present one at each SOF. This provides the programmability necessary for the Host Controller to synchronize with an external clocking resource and to adjust any unknown local clock offset.

Register 4-148: HcFrameInterval Register (UH0DR: Index 34h, Offset 534h)

Bit	Bit Definition	Bit Value	Value Definition
13:0	Frame Interval This specifies the interval between two consecutive SOFs in bit times. The nominal value is set to be 11,999. HCD should store the current value of this field before resetting HC. By setting the Host Controller Reset field of HcCommandStatus as this will cause the HC to reset this field to its nominal value. HCD may choose to restore the stored value upon the completion of the Reset sequence.		
15:14	Reserved		
30:16	Largest Data Packet This field specifies a value which is loaded into the Largest Data Packet Counter at the beginning of each frame. The counter value represents the largest amount of data in bits which can be sent or received by the HC in a single transaction at any given time without causing scheduling overrun. The field value is calculated by the HCD.		
31	FrameIntervalToggle HCD toggles this bit whenever it loads a new value to Frame Interval.		

The HcFrameRemaining register, a read-only register (see *Register 4-149*), is a 14-bit down counter showing the bit time remaining in the current Frame.

Register 4-149: HcFrameRemaining Register (UH0ER: Index 38h, Offset 538h)

Bit	Bit Definition	Bit Value	Value Definition
13:0	Frame Remaining This counter is decremented at each bit time. When it reaches zero, it is reset by loading the Frame Interval value specified in HcFmInterval at the next bit time boundary. When entering the USB Operational state, HC re-loads the content with the Frame Interval of HcFmInterval and uses the updated value from the next SOF.		
30:14	Reserved		
31	Frame Remaining Toggle This bit is loaded from the Frame Interval Toggle field of HcFmInterval whenever Frame Remaining reaches ‘0’. This bit is used by HCD for the synchronization between Frame Interval and Frame Remaining.		

The HcFrameNumber register, a read-only register (see *Register 4-150*), is a 16-bit counter. It provides a timing reference among events happening in the Host Controller and the Host Controller Driver. The Host Controller Driver may use the 16-bit value specified in this register and generate a 32-bit frame number without requiring frequent access to the register.

Register 4-150: HcFrameNumber Register (UH0FR: Index 3Ch, Offset 53Ch)

Bit	Bit Definition	Bit Value	Value Definition
15:0	Frame Number This is incremented when HcFmRemaining is re-loaded. It will be rolled over to 0h after ffffh. When entering the USBOPERATIONAL state, this will be incremented automatically. The content will be written to HCCA after HC has incremented the Frame Number at each frame boundary and sent a SOF but before HC reads the first ED in that Frame. After writing to HCCA, HC will set the Start of Frame in HcInterruptStatus.		
31:16	Reserved		

The HcPeriodicStart register, a read/write register (see *Register 4-151*), has a 14-bit programmable value which determines when is the earliest time HC should start processing the periodic list.

Register 4-151: HcPeriodicStart Register (UH10R: Index 40h, Offset 540h)

Bit	Bit Definition	Bit Value	Value Definition
13:0	Periodic Start After a hardware reset, this field is cleared. This is then set by HCD during the HC initialization. The value is calculated roughly as 10% off from HcFmInterval. A typical value will be 3E67h. When HcFmRemaining reaches the value specified, processing of the periodic lists will have priority over Control/Bulk processing. HC will therefore start processing the Interrupt list after completing the current Control or Bulk transaction that is in progress.		
31:14	Reserved		

The HcLowSpeedThreshold register, a read/write register (see *Register 4-152*), contains an 11-bit value used by the Host Controller to determine whether to commit to the transfer of a maximum of 8-byte LS packet before EOF. Neither the Host Controller nor the Host Controller Driver are allowed to change this value.

Register 4-152: HcLowSpeedThreshold Register (UH11R: Index 44h, Offset 544h)

Bit	Bit Definition	Bit Value	Value Definition
11:0	LS Threshold This field contains a value which is compared to the Frame Remaining field prior to initiating a Low Speed transaction. The transaction is started only if Frame Remaining ≥ this field. The value is calculated by HCD with the consideration of transmission and setup overhead.		
31:12	Reserved		

4.13.2. Root Hub Partition

All registers included in this partition are dedicated to the USB Root Hub which is an integral part of the Host Controller though still a functionally separate entity. The HCD emulates USBD accesses to the Root Hub via a register interface. The HCD maintains many USB-defined hub features which are not required to be supported in hardware. For example, the Hub's Device, Configuration, Interface, and Endpoint Descriptors are maintained only in the HCD as well as some static fields of the Class Descriptor. The HCD also maintains and decodes the Root Hub's device address as well as other trivial operations which are better suited to software than hardware.

The Root Hub register interface is otherwise developed to maintain similarity of bit organization and operation to typical hubs which are found in the system. Below are four register definitions: HcRhDescriptorA, HcRhDescriptorB, HcRhStatus, and HcRhPortStatus[1]. Each register is read and written as a Dword. These registers are only written during initialization to correspond with the system implementation. The HcRhDescriptorA and HcRhDescriptorB registers are implemented such that they are writeable regardless of the HC USB state. HcRhStatus and HcRhPortStatus will be writeable during the UsbOperational state.

The HcRhDescriptorA register (see *Register 4-153*) is the first register of two describing the characteristics of the Root Hub. The descriptor length (11), descriptor type TBD, and hub controller current (0) fields of the hub Class Descriptor are emulated by the HCD. All other fields are located in the HcRhDescriptorA and HcRhDescriptorB registers.

Register 4-153: HcRhDescriptorA Register (UH12R: Index 48h, Offset 548h)

Bit	Bit Definition	Bit Value	Value Definition
7:0	Number of Downstream Ports (Read Only) These bits specify the number of downstream ports supported by the Root Hub. This is set to 2as we support only 1 port.		
8	Power Switching Mode (R/W) This bit is used to specify how the power switching of the Root Hub ports is controlled. This field is only valid if the **No Power Switching** field is cleared. This bit can be programmed to either '0' or '1' since only one port is supported.	0	All ports are powered at the same time.
		1	Each port is powered individually. This mode allows port power to be controlled by either the global switch or per-port switching. If the **Port Power Control Mask** bit is set, the port responds only to port power commands (**Set/Clear Port Power**). If the port mask is cleared, then the port is controlled only by the global power switch (**Set/Clear Global Power**).
9	No Power Switching (R/W) These bits are used to specify whether power switching is supported or ports are always powered. When this bit is cleared, the **Power Switching Mode** specifies global or per-port switching. This bit can be programmed to '1' or '0' in our implementation since only one port is supported.	0	Ports are power switched
		1	Ports are always powered on when the HC is powered on.
10	Device Type This bit always return 0 indicating that the RootHub is not a compound device.		

Register 4-153: HcRhDescriptorA Register (UH12R: Index 48h, Offset 548h)

Bit	Bit Definition	Bit Value	Value Definition
11	Over Current Protection Mode (R/W) This bit describes how the overcurrent status for the Root Hub ports are reported. At reset, this fields should reflect the same mode as **Power Switching Mode**. This field is not valid since the **No Over Current Protection** field is set. This bit can be programmed to '1' or '0' in our implementation since only one port is supported.	0	Over-current status is reported collectively for all downstream ports.
		1	Over-current status is reported on a per-port basis.
12	No Over Current Protection (R/W) This bit can be programmed to '0' indicating that we support over current protection.	0	Over-current status is reported collectively for all downstream ports
		1	Over current protection is not supported.
23:13	Reserved		
31:24	Power On To Power Good Time (R/W) These bits specify the duration HCD has to wait before accessing a powered-on port of the Root Hub. The true value is this setting multiplied by 2ms.		

The HcRhDescriptorB register, a read/write register (see *Register 4-154*), is the second register of two describing the characteristics of the Root Hub. These fields are written during initialization to correspond with the system implementation.

Register 4-154: HcRhDescriptorB Register (UH13R: Index 4Ch, Offset 54Ch)

Bit	Bit Definition	Bit Value	Value Definition
15:0	Device Removable Each bit is dedicated to a port of the Root Hub. When cleared, the attached device is removable. When set, the attached device is not removable. Bit 0: Reserved Bit 1: Device attached to Port#1 Bit 2: Device attached to Port#2 Bits 3-15: N/A. Set to zero.		
31:16	Port Power Control Mask Each bit indicates if a port is affected by a global power control command when **Power Switching Mode** is set. When set, the port's power state is only affected by per-port power control (**Set/Clear Port Power**). When cleared, the port is controlled by the global power switch (**Set/Clear Global Power**). If the device is configured to global switching mode (**Power Switching Mode**=0), this field is not valid. Bit 0: Reserved Bit 1: Ganged-power mask on Port #1 Bit 2: Ganged-power mask on Port #2 Bits 3-15: N/A. Set to '0'		

The HcRhStatus register (see *Register 4-155*) is divided into two parts. The lower word of a Dword represents the Hub Status field and the upper word represents the Hub Status Change field. Reserved bits should always be written '0'.

Register 4-155: HcRhStatus Register (UH14R: Index 50h, Offset 550h)

Bit	Bit Definition	Bit Value	Value Definition
0	Local Power Status -- during Read (R/W) During Read this bit always returns 0. Clear Global Power – during Write In global power mode (Power Switching Mode=0), This bit is written to '1' to turn off power to all ports (clear Port Power Status). In per-port power mode, it clears Port Power Status only on ports whose Port Power Control Mask bit is not set. Writing a '0' has no effect.		
1	Over Current Indicator (Read Only) This bit reports over current conditions when the global reporting is implemented. When set, an over current condition exists. When cleared, all power operations are normal. If per-port over current protection is implemented this bit is always "0"		
14:2	Reserved		
15	Device Remote Wakeup Enable -- during Read (R/W) This bit enables a Connect Status Change bit as a resume event, causing a USBSUSPEND to USBRESUME state transition and setting the Resume Detected interrupt. Set Remote Wakeup Enable – during Write mode Writing a '1' sets Device Remote Wakeup Enable. Writing a '0' has no effect.	0 1	Connect Status Change is not a remote wakeup event. Connect Status Change is a remote wakeup event.
16	Local Power Status Change -- during Read (R/W) During Read this bit always returns '0'. Set Global Power – during Write In global power mode (**Power Switching Mode**=0), This bit is written to '1' to turn off power to all ports (clear **Port Power Status**). In per-port power mode, it sets **Port Power Status** only on ports whose **Port Power Control Mask** bit is not set. Writing a '0' has no effect.		
17	Over Current Indicator Change (R/W) This bit is set by Hardware when a change has occurred to the OCI field of this register. The HCD clears this bit by writing a '1'. Writing a '0' hs no effect.		
30:18	Reserved		
31	Clear Remote Wakeup Enable (W) Writing a '1' clears Device Remote Wakeup Enable. Writing a '0' has no effect.		

The HcRhPortStatus1 register, a read/write register (see *Register 4-156*), is used to control and report port events on Port #1. The lower word is used to reflect the port status, whereas the upper word reflects the status change bits. Some status bits are implemented with special write behavior (see below). If a transaction (token through handshake) is in progress when a write to change port status occurs, the resulting port status change must be postponed until the transaction completes. If HcRhStatus Register (UH14R: Index 50h, Offset 550h) needs to be set or reset then the reserved bits must be written '0'.

Register 4-156: HcRhPortStatus1 Register (UH15R: Index 54h, Offset 554h)

Bit	Bit Definition	Bit Value	Value Definition
0	Current Connect Status -- during read mode This bit reflects the current state of the downstream port. Clear Port Enable – during write mode The HCD writes a '1' to this bit to clear the Port Enable Status bit. Writing a '0' has no effect. The Current Connect Status is not affected by any write. Note: This bit is always read '1' when the attached device is nonremovable (Device Removeable[1]).	0	No device Connected
		1	Device Connected.
1	Port Enable Status -- during Read mode This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when an overcurrent condition, disconnect event, switched-off power, or operational bus error such as babble is detected. This change also causes Port Enabled Status Change to be set. HCD sets this bit by writing Set Port Enable and clears it by writing Clear Port Enable. This bit cannot be set when Current Connect Status is cleared. This bit is also set, if not already, at the completion of a port reset when Reset Status Change is set or port suspend when Suspend Status Change is set. Set Port Enable -- during Write Mode The HCD sets Port Enable Status by writing a '1'. Writing a '0' has no effect. If Current Connect Status is cleared, this write does not set Port Enable Status, but instead sets Connect Status Change. This informs the driver that it attempted to enable a disconnected port.	0	Port is Disabled
		1	Port is Enabled

Register 4-156: HcRhPortStatus1 Register (UH15R: Index 54h, Offset 554h)

Bit	Bit Definition	Bit Value	Value Definition
2	Port Suspend Status -- during Read mode This bit indicates the port is suspended or in the resume sequence. It is set by a Set Suspend State write and cleared when Port Suspend Status Change is set at the end of the resume interval. This bit cannot be set if Current Connect Status is cleared. This bit is also cleared when Port Reset Status Change is set at the end of the port reset or when the HC is placed in the USBRESUME state. If an upstream resume is in progress, it should propagate to the HC. Set Port Suspend -- during Write Mode The HCD sets the Port Suspend Status bit by writing a '1' to this bit. Writing a '0' has no effect. If Current Connect Status is cleared, this write does not set Port Suspend Status; instead it sets Connect Status Change. This informs the driver that it attempted to suspend a disconnected port.	0	Port is not suspended
		1	Port is suspended
3	Port Over Current Indicator -- during Read mode This bit is only valid when the Root Hub is configured in such a way that over current conditions are reported on a per-port basis. If per-port over current reporting is not supported, this bit is set to 0. If cleared, all power operations are normal for this port. If set, an over current condition exists on this port. This bit always reflects the over current input signal Clear Suspend Status -- during Write Mode The HCD writes a '1' to initiate a resume. Writing a '0' has no effect. A resume is initiated only if Port Suspend Status is set.	0	No Over current condition
		1	Over current condition detected on Port 1.
4	Port reset status -- during Read mode When this bit is set by a write to Set Port Reset, port reset signaling is asserted. When reset is completed, this bit is cleared when Port Reset Status Change is set. This bit cannot be set if Current Connect Status is cleared. Set Port Reset -- during Write Mode The HCD sets the port reset signaling by writing a '1' to this bit. Writing a '0' has no effect. If Current Connect Status is cleared, this write does not set Port Reset Status, but instead sets Connect Status Change. This informs the driver that it attempted to reset a disconnected port.	0	Port Reset signal is not active
		1	Port Reset signal is active
7:5	Reserved		

Register 4-156: HcRhPortStatus1 Register (UH15R: Index 54h, Offset 554h)

Bit	Bit Definition	Bit Value	Value Definition
8	Port Power status -- during Read mode This bit reflects the port's power status, regardless of the type of power switching implemented. This bit is cleared if an over-current condition is detected. HCD sets this bit by writing **Set Port Power** or **Set Global Power**. HCD clears this bit by writing **Clear Port Power** or **Clear Global Power**. Which power control switches are enabled is determined by **Power Switching Mode** and **Port Port Control Mask[1]**. In global switching mode (**Power Switching Mode**=0), only **Set/Clear Global Power** controls this bit. In per-port power switching (**Power Switching Mode**=1), if the **Port Power Control Mask[1]** bit for the port is set, only **Set/Clear Port Power** commands are enabled. If the mask is not set, only **Set/Clear Global Power** commands are enabled. When port power is disabled, **Current Connect Status**, **Port Enable Status**, **Port Suspend Status**, and **Port Reset Status** should be reset. Set Port power -- during Write Mode The HCD writes a '1' to set the **Port Power Status** bit. Writing a '0' has no effect. This bit is always reads '1' if power switching is not supported.	0	Port power is off
		1	Port power is on
9	Low Speed Device Attached -- during Read mode This bit indicates the speed of the device attached to this port. When set, a Low Speed device is attached to this port. When clear, a Full Speed device is attached to this port. This field is valid only when the **Current Connect Status** is set. Clear Port power -- during Write Mode The HCD clears the **Port Power Status** bit by writing a '1'. Writing a '0' has no effect.	0	Full speed device attached
		1	Low speed device attached
15:10	Reserved		

Register 4-156: HcRhPortStatus1 Register (UH15R: Index 54h, Offset 554h)

Bit	Bit Definition	Bit Value	Value Definition
16	Connect Status Change This bit is set whenever a connect or disconnect event occurs. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. If **Current Connect Status** is cleared when a **Set Port Reset, Set Port Enable**, or **Set Port Suspend** write occurs, this bit is set to force the driver to re-evaluate the connection status since these writes should not occur if the port is disconnected. If the **Device Removable[1]** bit is set, this bit is set only after a Root Hub reset to inform the system that the device is attached.	0	No change in Current Connect Status
		1	change in Current Connect Status
17	Port Enable Status Change This bit is set when hardware events cause the **Port Enable Status** bit to be cleared. Changes from HCD writes do not set this bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect.	0	No change in Port Enable Status
		1	change in Port Enable Status
18	Port Suspend Status Change This bit is set when the full resume sequence has been completed. This sequence includes the 20ms resume pulse, LS EOP, and 3-ms resychronization delay. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. This bit is also cleared when **Reset Status Change** is set.	0	Resume is not completed
		1	Resume is completed
19	Port Over Current Indicator Change This bit is valid only if over current conditions are reported on a per-port basis. This bit is set when Root Hub changes the **Port Over Current Indicator** bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect.	0	No change in Port Over Current Indicator
		1	Port Over Current Indicator has changed
20	Port Reset Status Change This bit is set at the end of the 10-ms port reset signal. The HCD writes a '1' to clear this bit. Writing a '0' has no effect.	0	Port Reset is not completed
		1	Port Reset is completed
31:21	Reserved		

The HcRhPortStatus2 register, a read/write register (see), is used to control and report port events on Port #2. The lower word is used to reflect the port status, whereas the upper word reflects the status change bits. Some status bits are implemented with special write behavior (see below). If a transaction (token through handshake) is in progress when a write to change port status occurs, the resulting port status change must be postponed until the transaction completes. Reserved bits should always be written as '0'.

Register 4-157: HcRhPortStatus2 Register (UH16R: Index 58h, Offset 558h)

Bit	Bit Definition	Bit Value	Value Definition
0	Current Connect Status -- during read mode This bit reflects the current state of the down-stream port. Clear Port Enable – during write mode The HCD writes a '1' to this bit to clear the Port Enable Status bit. Writing a '0' has no effect. The Current Connect Status is not affected by any write. This bit is always read '1' when the attached device is nonremovable (Device Remove-able[1]).	0	No device Connected
		1	Device Connected.
1	Port Enable Status -- during Read mode This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when an overcurrent condition, disconnect event, switched-off power, or operational bus error such as babble is detected. This change also causes Port Enabled Status Change to be set. HCD sets this bit by writing Set Port Enable and clears it by writing Clear Port Enable. This bit cannot be set when Current Connect Status is cleared. This bit is also set, if not already, at the completion of a port reset when Reset Status Change is set or port suspend when Suspend Status Change is set. Set Port Enable -- during Write Mode The HCD sets Port Enable Status by writing a '1'. Writing a '0' has no effect. If Current Connect Status is cleared, this write does not set Port Enable Status, but instead sets Con-nect Status Change. This informs the driver that it attempted to enable a disconnected port.	0	Port is Disabled
		1	Port is Enabled

Register 4-157: HcRhPortStatus2 Register (UH16R: Index 58h, Offset 558h)

Bit	Bit Definition	Bit Value	Value Definition
2	Port Suspend Status -- during Read mode This bit indicates the port is suspended or in the resume sequence. It is set by a Set Suspend State write and cleared when Port Suspend Status Change is set at the end of the resume interval. This bit cannot be set if Current Connect Status is cleared. This bit is also cleared when Port Reset Status Change is set at the end of the port reset or when the HC is placed in the USBRESUME state. If an upstream resume is in progress, it should propagate to the HC. Set Port Suspend -- during Write Mode The HCD sets the Port Suspend Status bit by writing a '1' to this bit. Writing a '0' has no effect. If Current Connect Status is cleared, this write does not set Port Suspend Status; instead it sets Connect Status Change. This informs the driver that it attempted to suspend a disconnected port.	0	Port is not suspended
		1	Port is suspended
3	Port Over Current Indicator -- during Read mode This bit is only valid when the Root Hub is configured in such a way that over current conditions are reported on a per-port basis. If per-port over current reporting is not supported, this bit is set to 0. If cleared, all power operations are normal for this port. If set, an over current condition exists on this port. This bit always reflects the over current input signal Clear Suspend Status -- during Write Mode The HCD writes a '1' to initiate a resume. Writing a '0' has no effect. A resume is initiated only if Port Suspend Status is set.	0	No Over current condition
		1	Over current condition detected on Port 1.
4	Port reset status -- during Read mode When this bit is set by a write to Set Port Reset, port reset signaling is asserted. When reset is completed, this bit is cleared when Port Reset Status Change is set. This bit cannot be set if Current Connect Status is cleared. Set Port Reset -- during Write Mode The HCD sets the port reset signaling by writing a '1' to this bit. Writing a '0' has no effect. If Current Connect Status is cleared, this write does not set Port Reset Status, but instead sets Connect Status Change. This informs the driver that it attempted to reset a disconnected port.	0	Port Reset signal is not active
		1	Port Reset signal is active
7:5	Reserved		

Register 4-157: HcRhPortStatus2 Register (UH16R: Index 58h, Offset 558h)

Bit	Bit Definition	Bit Value	Value Definition
8	Port Power status -- during Read mode This bit reflects the port's power status, regardless of the type of power switching implemented. This bit is cleared if an over-current condition is detected. HCD sets this bit by writing **Set Port Power** or **Set Global Power**. HCD clears this bit by writing **Clear Port Power** or **Clear Global Power**. Which power control switches are enabled is determined by **Power Switching Mode** and **Port Port Control Mask[1]**. In global switching mode (**Power Switching Mode**=0), only **Set/Clear Global Power** controls this bit. In per-port power switching (**Power Switching Mode**=1), if the **Port Power Control Mask[1]** bit for the port is set, only **Set/Clear Port Power** commands are enabled. If the mask is not set, only **Set/Clear Global Power** commands are enabled. When port power is disabled, **Current Connect Status**, **Port Enable Status**, **Port Suspend Status**, and **Port Reset Status** should be reset. Set Port power -- during Write Mode The HCD writes a '1' to set the **Port Power Status** bit. Writing a '0' has no effect. This bit is always reads '1' if power switching is not supported.	0	Port power is off
		1	Port power is on
9	Low Speed Device Attached -- during Read mode This bit indicates the speed of the device attached to this port. When set, a Low Speed device is attached to this port. When clear, a Full Speed device is attached to this port. This field is valid only when the **Current Connect Status** is set. Clear Port power -- during Write Mode The HCD clears the **Port Power Status** bit by writing a '1'. Writing a '0' has no effect.	0	Full speed device attached
		1	Low speed device attached
15:10	Reserved (Read Only) These bits always return '0'		

Register 4-157: HcRhPortStatus2 Register (UH16R: Index 58h, Offset 558h)

Bit	Bit Definition	Bit Value	Value Definition
16	Connect Status Change This bit is set whenever a connect or disconnect event occurs. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. If **Current Connect Status** is cleared when a **Set Port Reset, Set Port Enable**, or **Set Port Suspend** write occurs, this bit is set to force the driver to re-evaluate the connection status since these writes should not occur if the port is disconnected. If the **Device Removable[1]** bit is set, this bit is set only after a Root Hub reset to inform the system that the device is attached.	0	No change in Current Connect Status
		1	change in Current Connect Status
17	Port Enable Status Change This bit is set when hardware events cause the **Port Enable Status** bit to be cleared. Changes from HCD writes do not set this bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect.	0	No change in Port Enable Status
		1	change in Port Enable Status
18	Port Suspend Status Change This bit is set when the full resume sequence has been completed. This sequence includes the 20ms resume pulse, LS EOP, and 3-ms resychronization delay. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. This bit is also cleared when **Reset Status Change** is set.	0	Resume is not completed
		1	Resume is completed
19	Port Over Current Indicator Change This bit is valid only if over current conditions are reported on a per-port basis. This bit is set when Root Hub changes the **Port Over Current Indicator** bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect.	0	No change in Port Over Current Indicator
		1	Port Over Current Indicator has changed
20	Port Reset Status Change This bit is set at the end of the 10-ms port reset signal. The HCD writes a '1' to clear this bit. Writing a '0' has no effect.	0	Port Reset is not completed
		1	Port Reset is completed
31:21	Reserved		

4.14 Serial Peripheral Interface Module (MQ-1132 only)

The MQ-1132 interfaces to an SPI compliant device that is a synchronous serial bus. Data transfer for the SPI Module is provided in either one or the other of the following ways:

- full-duplex mode of data transfer using three pins
- or half-duplex mode of data transfer using two pins

The minimum number of pins required to realize the Master Mode functionality on the SPI interface are three. The SPI Module can be configured to operate either in Master Mode or Slave Mode. SS# pin is used to indicate a multi-master bus contention that is explained later when the SPI Module is in Master mode or a Slave Select Pin when the SPI Module is in Slave Mode.

The SPI Peripheral Interface Module can also be programmed to operate in GPIO mode in which case all the pins allocated for the SPI functionality explained later act as General Purpose I/Os.

In order to realize the SPI functionality in the MQ-1132 and support both Master Mode as well as the Slave Mode of operation, the pins listed in are required.

Register 4-158: Pins Required for SPI

Signal	Description
MISO	**Master In, Slave Out – Data Pin** In case the SPI Module internal to the MQ-1132 is programmed to operate in SPI Mode of Operation in Master Mode, this pin is used as receive pin to serially shift-in the data. In case the SPI Module internal to the MQ-1132 is programmed to operate in SPI Mode of Operation in Slave Mode, this pin is used as a transmit pin to Serially shift-out the data.
MOSI	**Master Out, Slave In – Data Pin** In case the SPI Module internal to the MQ-1132 is programmed to operate in SPI Mode of Operation in Master Mode, this pin is used as transmit pin to serially shift-out the data. In case the SPI Module internal to the MQ-1132 is programmed to operate in SPI Mode of Operation in Slave Mode, this pin is used as receive pin to Serially shift-in the data.
SCK	**Serial Clock – Clock Pin** In case the SPI Module internal to the MQ-1132 is programmed to be in SPI Mode of Operation in Master Mode, this pin is in the output mode and is used to drive the Serial Clock to all the Slave devices. Receive and transmit data are sampled based on this clock. In case the SPI Module internal to the MQ-1132 is programmed to be in SPI Mode of Operation in Slave Mode, this pin is in input mode and is used to receive the clock driven by a master in the system.
SS#	**Slave Select pin** In case the SPI Module internal to the MQ-1132 is programmed to be in SPI Mode of Operation in Master Mode, this pin can be optionally used to indicate multiple-master bus contention in which case this pin becomes input. In case the mode of operation is set to be in Master Mode and the Mode fault detection is disabled, this pin is an output and is used to generate Slave Select Signal that toggles for every data transfer in CPHA=0 type of transfer format. In case the SPI Module internal to the MQ-1132 is programmed to be in SPI Mode of Operation in Slave Mode, this pin provides the functionality of selecting the MQ-1132 as a slave device.

Based on the above pins, it is clear that the Serial Peripheral Interface Module provides the capability to transmit (Shift-Out Serially) and receive (Shift-in Serially) data on the MOSI and MISO pins. The Serial Clock SCK is used to synchronize sampling of the information that is available on the two serial data lines and also shift-in or shift-out the data into or out of the respective shift registers. The Slave devices that are not selected due to the de-assertion of their respective Slave Select pins SS#, do not drive the Serial Peripheral interface bus.

The SPI Module can perform a serial data transfer of data size equal to 8 or 16 bits. The programmability is provided to either transfer the Most Significant Bit or the Least Significant bit of a particular data transfer as the beginning bit. Based on the SPI Specifications provided by Motorola, the serial data transfers are performed in two different formats classified as follows:

1. CPHA = 0 Transfer Format: Clock Phase is equal to zero. The Clock Polarity can be equal to 0 or 1.
2. CPHA = 1 Transfer Format: Clock Phase is equal to one. The Clock Polarity can be equal to 0 or 1.

The SPI Module is designed to support both the above transfer formats. When the SPI Module is configured as a Master, adequate flexibility is provided to have different frequencies of the Serial Clock.

The following register set is required to use the SPI Module:

- SPI Module Control Register (SPIMCR)
- SPI Module Status Register (SPIMSR)
- SPI Module Time Gap Compare Register (SPIMTGR)
- SPI Module Data Register (SPIMDR)
- SPI Module GPIO Direction/Data Register.(SPIMGPIO)
- SPI Module Data Count Register (SPIRDCR)
- SPI Module FIFO Threshold Register (SPIMFTHR)
- LED Module Control Register (LEDCR)
- General Purpose I/O Register (BLUMGPR)

4.14.1. Transmit Operation

All the write operations performed to the SPIMDR Register results in a write operation to the Transmit FIFO. In case the SPI Module is in 8-bit Mode of operation, the transmit FIFO is configured as an 8-bit Wide by 64 Deep FIFO. In case the SPI Module is configured to operate in 16-bit mode, the Transmit FIFO is configured as 16-bit Wide by 32 deep FIFO. In case the user would like to transfer only one byte/word at a time and transmit the next byte/word only after the successful transmission of the first byte/word, the user can enable single transfer mode. In the case of single transfer mode, the user gets an interrupt after the successful transmission of one byte/word. In the case of continuous transfer mode and in master mode, the data in transmit FIFO is read by the transmit logic and one byte/word of data is transmitted at a time with a pre-programmed delay between each transfer. The delay is programmed in the Time Gap Compare register. A counter starts counting based on SCK clock at the end of the data transfer and when the value is greater than the contents of the Time Gap Compare register, the second data transfer is triggered, provided, there is data in the transmit FIFO. It is important to note that a write into the Transmit FIFO is required to trigger a SPI data transfer to support the above modes of operation.

Based on the system requirements, sometimes it is desirable to only receive data. In this case, it is not necessary to write to the transmit FIFO. Instead, the host can program a required count value into the SPIRDCR register and initiate a SPI Transfer Without write into the transmit FIFO by setting SPIMCR[31]. The count value in this case can be a maximum of 64 in the 8-bit mode of operation and can be 32 in the 16-bit mode of operation. The host can also do a continuous data transfer where the count value is ignored and the transfer can be aborted by the software by disabling SPIRDCR[7].

4.14.2. Receive Operation

All the read operations performed from the SPIMDR register results in a read operation from the receive FIFO. When the receive function is enabled, the serial data on the receive pin is shifted into the Serial-IN Parallel-OUT (SIPO) shift register. Once the required size of data is received on the Receive line, it is written into the Receive FIFO. The user can be interrupted whenever a data is received in the receive FIFO. In case the SPI module is programmed to operate in Master Mode, the interval between each data transfer is governed by the value programmed in the Time Gap Compare Register. In case the SPI module is programmed as a slave, there might be certain requirements with respect to the minimum interval between two successive data transfers based on the interrupt response time and the FIFO depth provided.

Table 4-15 specifies the index, offset and reset values for host controller operation registers.

TABLE 4-15: SPI Register Index and Reset Values

Register	Index	Offset	Reset Value	See Description
SP00R	00h	300h	0000-0000h	*Register 4-159 on page 193*
SP01R	04h	304h	0000-0000h	*Register 4-160 on page 197*
SP02R	08h	308h	0000-0000h	*Register 4-161 on page 203*
SP03R	0Ch	30Ch	0000-0000h	*Register 4-162 on page 203*
SP04R	10h	310h	0000-0000h	*Register 4-163 on page 203*
SP05R	14h	314h	0000-0000h	*Register 4-164 on page 205*
SP06R	18h	318h	0000-0000h	*Register 4-165 on page 206*
SP07R	1Ch	31Ch	0000-0000h	*Register 4-166 on page 210*
SP08R	20h	320h	0000-0000h	*Register 4-167 on page 212*

Register 4-159 through *Register 4-167 on page 212* specify the SPI registers.

Register 4-159: SPI Module Control Register (SP00R: Index 00h, Offset 300h)

Bit	Bit Definition	Bit Value	Value Definition
1:0	SPI Mode Enable Bits. These two bits are used to program the mode of operation of the SPI Module. On power on, the SPI Pins MOSI, SCK and SS come up as outputs and MISO comes up as input (GPIO Mode). A value of 01 implies, the mode of operation of the SPI Module is in SPI Mode. A value of 10, which is test mode 1, routes specific signals to the output. When the Test Mode 2 is enabled, some of the counters internal to the SPI Module logic can be accessed directly to provide assistance in increasing the fault coverage.	00	GPIO Mode is enabled.
		01	SPI Mode is enabled.
		10	Test mode 1 enabled.
		11	Test mode 2 enabled.
2	R/W. Master or Slave Mode Select Bit. The software can configure the SPI Module internal to the MQ-1132 in Master Mode or Slave Mode.	0	SPI Module is in Master Mode.
		1	SPI Module is in Slave Mode.
3	R/W. Serial Data Ordering Bit. The software can configure this bit in the SPI Module internal to the MQ-1132 to start a serial data transfer with either LSB or MSB as the first bit of a byte or word that is transferred.	0	The LSB is the first bit transferred.
		1	The MSB is the first bit transferred.

Register 4-159: SPI Module Control Register (SP00R: Index 00h, Offset 300h)

Bit	Bit Definition	Bit Value	Value Definition
4	R/W. Data Transfer Size. The software can configure the SPI Module internal to the MQ-1132 to transfer either a Byte (8 bits) or a Word (16 bits) of data.	0	Transfer Size is a byte (8 bits).
		1	Transfer Size is a word (16 bits).
5	R/W. Serial Clock (SCK) Polarity. The software can configure the SPI Module internal to the MQ-1132 to select the inactive state of the SCK line. This bit is used in conjunction with the Clock Phase bit (SPIMCR [6]) to implement the two different types of data transfer formats between the Master and the Slave devices.	0	The SCK pin is at logic level '0' when inactive.
		1	The SCK pin is at logic level '1' when inactive.
6	R/W. Serial Clock (SCK) Phase. The software can configure the SPI Module internal to the MQ-1132 to select the clock edge that is used to change the data and the clock edge that is used to sample the data. This bit is used in conjunction with the SCK Polarity bit (SPIMCR [5]) to implement the two different types of data transfer formats.	0	Data is sampled off of the Leading Edge and the data changes off of the Trailing Edge of SCK.
		1	Data is sampled off of the Trailing Edge and the data changes off of the Leading Edge of SCK.
7	R/W. SPI Transmit Function Enable Bit. This bit is used to enable or disable the Transmit PAD.	0	Transmit PAD disabled.
		1	Transmit PAD Enabled.
8	R/W. SPI Receive Function Enable Bit. The software can configure the SPI Module internal to the MQ-1132 to either enable or disable the receive operation. In case the Receive function is disabled, no data is sampled on the Receive line.	0	Receive Function Disabled.
		1	Receive Function Enabled.
9	R/W. SPI Transfer Mode Select Bit The software can configure the SPI Module internal to the MQ-1132 to operate in Single Transfer Mode or Continuous Transfer Mode. In the case of Single Transfer Mode, the SPI Transfer complete signal is set after every data transfer. In the Continuous Transfer Mode, the SPI Transfer Complete Signal is set after transferring all the data inside the Transmit FIFO.	0	Single Transfer Mode Enabled.
		1	Continuous Transfer Mode Enabled.
10	R/W. SPI Interrupt Enable Bit. The software can configure the SPI Module internal to the MQ-1132 to interrupt the processor whenever the SPI reaches the end of the transmission (SPI Transfer Complete Bit is set) or a Mode fault occurred or some FIFO threshold related conditions get set. This interrupt is cleared when the appropriate bits in the SPIMSR are cleared that caused the interrupt.	0	Interrupt is disabled.
		1	Interrupt is enabled.

Register 4-159: SPI Module Control Register (SP00R: Index 00h, Offset 300h)

Bit	Bit Definition	Bit Value	Value Definition
14:11	Clock Divider – First Level pre-divider Logic The SCK Clock is derived off either the oscillator clock or the bus clock. Clock output is pre-divided based on these bits to generate a PDCLK.	0000	Divided by 1.
		0001	Divided by 2.
		0010	Divided by 3.
		0011	Divided by 4.
		0100	Divided by 5.
		0101	Divided by 6.
		0110	Divided by 7.
		0111	Divided by 8.
		1000	Divided by 9.
		1001	Divided by 10.
		1010	Divided by 11.
		1011	Divided by 12.
		1100	Divided by 13.
		1101	Divided by 14.
		1110	Divided by 15.
		1111	Divided by 16.
18:15	Clock Divider – Second Level post-divider logic The Timer counts down from the maximum value based on the clock devide or the Bus Clock based on the setting of SP04R[22]. This clock is further divided based on the setting of these bits.	0000	Divided by 1.
		0001	Divided by 2.
		0010	Divided by 3.
		0011	Divided by 4.
		0100	Divided by 5.
		0101	Divided by 6.
		0110	Divided by 7.
		0111	Divided by 8.
		1000	Divided by 9.
		1001	Divided by 10.
		1010	Divided by 11.
		1011	Divided by 12.
		1100	Divided by 13.
		1101	Divided by 14.
		1110	Divided by 15.
		1111	Divided by 16.
19	R/W. Transfer Complete Mask Bit. This bit controls the masking of the interrupt caused when a transfer is completed.	0	SPI Transfer complete masked.
		1	SPI Transfer complete not masked.
20	R/W. Fault Mode Mask Bit. This bit controls the masking of the interrupt caused when a fault occurs due to the assertion of the Slave Select pin of the MQ-1132 when SPI Module internal to the MQ-1132 is programmed to be in Master Mode and it is transmitting.	0	Fault masked.
		1	Fault not masked.
21	R/W. Transmit FIFO Threshold Interrupt Mask Bit. This bit controls the masking of the interrupt caused when the Transmit FIFO reaches a desired threshold value mentioned in the FIFO Threshold Register.	0	Transmit FIFO Threshold Interrupt masked.
		1	Transmit FIFO Threshold Interrupt not masked.

Register 4-159: SPI Module Control Register (SP00R: Index 00h, Offset 300h)

Bit	Bit Definition	Bit Value	Value Definition
22	R/W. SPI Transfer Enable –**By Writing to the Data Register**. (SPI transfer initiated by writing to the Data Register (Transmit FIFO)) This bit enables the SPI Transfer. The software sets this bit when it is desired to initiate a data transfer by writing into the Data Register. For both Continuous and Single transfer mode, this bit is applicable.	0	SPI Transfer Disabled.
		1	SPI Transfer is Enabled.
23	R/W. Transmit FIFO Software reset. This bit is set by the software to reset the Transmit FIFO.	0	Software reset for Transmit FIFO Disabled.
		1	Software reset for Transmit FIFO Enabled.
24	R/W. Receive FIFO Software reset. This bit is set by the software to reset the Receive FIFO.	0	Software reset for Receive FIFO Disabled.
		1	Software reset for Receive FIFO Enabled.
25	R/W. Receive FIFO Threshold Interrupt Mask Bit. This bit controls the masking of the interrupt caused when the Receive FIFO reaches a desired threshold value mentioned in the FIFO Threshold Register.	0	Receive FIFO Threshold Interrupt masked.
		1	Receive FIFO Threshold Interrupt not masked.
26	R/W. Receive FIFO Overflow Interrupt Mask Bit (Applicable in Slave Mode of Operation). This bit controls the masking of the interrupt caused when the Receive FIFO overflows. This is useful in Slave mode to trigger an error condition.	0	Receive FIFO Overflow Interrupt masked.
		1	Receive FIFO Overflow Interrupt not masked.
27	R/W. Transmit FIFO Underflow Interrupt Mask Bit (Applicable in Slave Mode of operation). This bit controls the masking of the interrupt caused when the Transmit function is enabled and the SCK clock is driven by an external master and the transmit FIFO is empty. This triggers an error condition.	0	Transmit FIFO Underflow Interrupt masked.
		1	Transmit FIFO Underflow Interrupt not masked.
29:28	Reserved		
30	R/W. Mode selection bit for SS Pin. When the Mode of operation is set to SPI Mode this bit decides whether SS Pin is a true SS Pin (controlled by SPI Module) or GPO (controlled by software).	0	SS Pin is a true SS Pin and is controlled by SPI Module.
		1	SS Pin is a GPO and the value written in the register bit SPIMGPIO [3] is driven on to this Pin.

Register 4-159: SPI Module Control Register (SP00R: Index 00h, Offset 300h)

Bit	Bit Definition	Bit Value	Value Definition
31	R/W. SPI Transfer Enable Bit –Without writing to the Data register. This bit is used to trigger a SPI Transfer operation and overrides the triggering of the transfer operation based on writes to the Transmit FIFO (Data Register). This feature is provided to receive the data continuously or based on the count value programmed in the SPIRDCR register with SPIRDCR [7] set to 0. While receive transfer is in progress, in case transmit FIFO is not empty, the data is read from the transmit FIFO and transmitted. This bit is set only after writing a meaningful value into SPIRDCR register. On power on, this bit comes up as disabled = 0. Software sets this bit to 1 to indicate transfer enable.		

Register 4-160: SPI Module Status Register (SP01R: Index 04h, Offset 304h)

Bit	Bit Definition	Bit Value	Value Definition
0	R/W. Transfer Status Bit. This bit indicates whether a transfer has been completed. Only the SPI Module sets this bit. Writing a 1 can clear this bit. The bits SPIMCR [10] and bit SPIMCR [19] must be set to one.	0	SPI Transfer in progress.
		1	SPI Transfer is completed.
1	R/W. Fault Mode Condition Bit. In case the SPI Module internal to the MQ-1132 has been programmed to operate in Master Mode and some other SPI compliant device in the system tries to drive the MQ-1132's Slave Select Signal, this bit is set. Writing a 1 can clear this bit. The bits SPIMCR [10] and SPIMCR [20] must be set to one.	0	No Fault Mode is detected.
		1	Fault Mode is detected.
2	R/W. Transmit FIFO Threshold Bit. This bit is set when the Transmit FIFO has reached the desired threshold and bit SPIMCR [10] and bit SPIMCR [21] must be set to 1.	0	Transmit FIFO Threshold Interrupt – False
		1	Transmit FIFO Threshold Interrupt – True
5:3	Reserved		
6	R/W. Receive FIFO Threshold Bit. This bit is set when the Receive FIFO has reached the desired threshold and the Mask Bit SPIMCR [25] is set. Writing a 1 can clear this bit.The bits SPIMCR [10] and SPIMCR [25] must be set to one.	0	Receive FIFO Threshold – False
		1	Receive FIFO Threshold – True

Register 4-160: SPI Module Status Register (SP01R: Index 04h, Offset 304h)

Bit	Bit Definition	Bit Value	Value Definition
7	R/W. Receive FIFO Overflow Bit. (Applicable in Slave Mode Operation) This bit is set when the Receive function is enabled with the Mask bit SPIMCR [26] set and the receive data is sampled on the receive line while the receive FIFO is full. Writing a 1 can clear this bit. This is useful in Slave mode of operation to trigger an error condition.The bits SPIMCR [10] and SPIMCR [26] must be set to one.	0	Receive FIFO Overflow – False
		1	Receive FIFO Overflow – True
8	R/W. Transmit FIFO Underflow Bit (Applicable in Slave Mode Operation) This bit is set when the Transmit function is enabled with the Mask bit SPIMCR [27] set and the external master drives the clock and the Transmit FIFO is empty. This is useful in Slave mode of operation to trigger an error condition. The bits SPIMCR [10] and SPIMCR [27] must be set to one.	0	Transmit FIFO Underflow – False
		1	Transmit FIFO Underflow – True

Register 4-160: SPI Module Status Register (SP01R: Index 04h, Offset 304h)

Bit	Bit Definition	Bit Value	Value Definition
15:9	Read Only. Transmit FIFO Status Bits These bits can be read by the host and indicate the number of locations free in the Transmit FIFO. The Transmit FIFO is configured as 64 deep FIFO in 8-bit mode of SPI operation and as a 32 deep FIFO in 16-bit mode of SPI operation. In both the modes of operation, a value of 7'b00000000 implies the FIFO is Full. In 16-bit Mode, a value of 7'b01000000 implies the FIFO is empty.	0000000	Transmit FIFO is Full
		0000001	1 location available.
		0000010	2 locations available.
		0000011	3 locations available.
		0000100	4 locations available.
		0000101	5 locations available.
		0000110	6 locations available.
		0000111	7 location available.
		0001000	8 locations available.
		0001001	9 locations available.
		0001010	10 locations available.
		0001011	11 locations available.
		0001100	12 locations available
		0001101	13 locations available.
		0001110	14 locations available.
		0001111	15 locations available.
		0010000	16 locations available
		0010001	17 location available.
		0010010	18 locations available.
		0010011	19 locations available.
		0010100	20 locations available.
		0010101	21 locations available.
		0010110	22 locations available.
		0010111	23 location available.
		0011000	24 locations available.
		0011001	25 locations available.
		0011010	26 locations available.
		0011011	27 locations available.
		0011100	28 locations available
		0011101	29 locations available.
		0011110	30 locations available.
		0011111	31 locations available.
		0100000	32 locations available. (Transmit FIFO Empty - for 16-bit mode of SPI Operation)

Descriptions of Bits 15:9 are continued on the next page.

Register 4-160: SPI Module Status Register (SP01R: Index 04h, Offset 304h)

Bit	Bit Definition	Bit Value	Value Definition
15:9	Read Only. Transmit FIFO Status Bits These bits can be read by the host and indicate the number of locations free in the Transmit FIFO. The Transmit FIFO is configured as 64 deep FIFO in 8-bit mode of SPI operation and as a 32 deep FIFO in 16-bit mode of SPI operation. In both the modes of operation, a value of 7'b00000000 implies the FIFO is Full. In 16-bit Mode, a value of 7'b01000000 implies the FIFO is empty.	0100001	33 location available.
		0100010	34 locations available.
		0100011	35 locations available.
		0100100	36 locations available.
		0100101	37 locations available.
		0100110	38 locations available.
		0100111	39 location available.
		0101000	40 locations available.
		0101001	41 locations available.
		0101010	42 locations available.
		0101011	43 locations available.
		0101100	44 locations available
		0101101	45 locations available.
		0101110	46 locations available.
		0101111	47 locations available.
		0110000	48 locations available
		0110001	49 location available.
		0110010	50 locations available.
		0110011	51 locations available.
		0110100	52 locations available.
		0110101	53 locations available.
		0110110	54 locations available.
		0110111	55 location available.
		0111000	56 locations available.
		0111001	57 locations available.
		0111010	58 locations available.
		0111011	59 locations available.
		0111100	60 locations available
		0111101	61 locations available.
		0111110	62 locations available.
		0111111	63 locations available.
		1000000	Transmit FIFO is empty.

Register 4-160: SPI Module Status Register (SP01R: Index 04h, Offset 304h)

Bit	Bit Definition	Bit Value	Value Definition
22:16	Read Only. Receive FIFO Status. These bits can be read by the host and indicate the number of locations free in the Receive FIFO. The Receive FIFO is configured as 64 deep FIFO in 8-bit mode of SPI operation and as a 32 deep FIFO in 16-bit mode of SPI operation. In both the modes of operation, a value of 7'b00000000 implies the FIFO is Full. In 16-bit Mode, a value of 7'b01000000 implies the FIFO is empty.	0000000	Receive FIFO is Full
		0000001	1 location available.
		0000010	2 locations available.
		0000011	3 locations available.
		0000100	4 locations available.
		0000101	5 locations available.
		0000110	6 locations available.
		0000111	7 location available.
		0001000	8 locations available.
		0001001	9 locations available.
		0001010	10 locations available.
		0001011	11 locations available.
		0001100	12 locations available
		0001101	13 locations available.
		0001110	14 locations available.
		0001111	15 locations available.
		0010000	16 locations available
		0010001	17 location available.
		0010010	18 locations available.
		0010011	19 locations available.
		0010100	20 locations available.
		0010101	21 locations available.
		0010110	22 locations available.
		0010111	23 location available.
		0011000	24 locations available.
		0011001	25 locations available.
		0011010	26 locations available.
		0011011	27 locations available.
		0011100	28 locations available
		0011101	29 locations available.
		0011110	30 locations available.
		0011111	31 locations available.
		0100000	32 locations available. (Receive FIFO Empty – for 16-bit mode of SPI Operation)
Descriptions of Bits 22:16 are continued on the next page.			

Register 4-160: SPI Module Status Register (SP01R: Index 04h, Offset 304h)

Bit	Bit Definition	Bit Value	Value Definition
22:16	Read Only. Receive FIFO Status. These bits can be read by the host and indicate the number of locations free in the Receive FIFO. The Receive FIFO is configured as 64 deep FIFO in 8-bit mode of SPI operation and as a 32 deep FIFO in 16-bit mode of SPI operation. In both the modes of operation, a value of 7'b00000000 implies the FIFO is Full. In 16-bit Mode, a value of 7'b01000000 implies the FIFO is empty.	0100001	33 location available.
		0100010	34 locations available.
		0100011	35 locations available.
		0100100	36 locations available.
		0100101	37 locations available.
		0100110	38 locations available.
		0100111	39 location available.
		0101000	40 locations available.
		0101001	41 locations available.
		0101010	42 locations available.
		0101011	43 locations available.
		0101100	44 locations available
		0101101	45 locations available.
		0101110	46 locations available.
		0101111	47 locations available.
		0110000	48 locations available
		0110001	49 location available.
		0110010	50 locations available.
		0110011	51 locations available.
		0110100	52 locations available.
		0110101	53 locations available.
		0110110	54 locations available.
		0110111	55 location available.
		0111000	56 locations available.
		0111001	57 locations available.
		0111010	58 locations available.
		0111011	59 locations available.
		0111100	60 locations available
		0111101	61 locations available.
		0111110	62 locations available.
		0111111	63 locations available.
		1000000	Receive FIFO is empty.
31:23	Reserved		

Register 4-161: SPI Module Data Register (SP02R: Index 08h, Offset 308h)

Bit	Bit Definition	Bit Value	Value Definition
7:0	R/W. Data Register – Lower Byte In 8-bit transfer mode, this lower byte contains the actual data. The MSB in 8-bit transfer mode is SPIMDR [7]. In 16-bit transfer mode, this lower byte holds the least significant 8-bits of data. A Read operation to these bits result in a read of the Lower Byte from the receive FIFO. A Write operation to these bits results in a write to the Lower Byte of the Transmit FIFO.		
15:8	R/W. Data Register– Upper Byte In 16-bit transfer mode, this upper byte contains the most significant 8-bits of actual data. In 16-bit transfer mode, SPIMDR [15] is the MSB of a 16-bit data transferred. A Read operation to these bits result in a read of the Upper Byte from the receive FIFO. A Write operation to these bits results in a write to the Upper Byte of the Transmit FIFO.		
31:16	Reserved		

Register 4-162: SPI Module Time Gap Compare Register (SP03R: Index 0Ch, Offset 30Ch)

Bit	Bit Definition	Bit Value	Value Definition
15:0	R/W. Delay Count Register In case the SPI module is programmed to operate master mode, the time between each data transfer is greater than ((SCK clock time period) X (the contents of this register)). This time gap feature is valid when the SPI Module is programmed to operate in following modes: Continuous Mode of operation with the data transfer initiated by writing into the Data Register (Transmit FIFO). Fixed and continuous mode of operation that is achieved by setting SPIMCR [31].		
31:16	Reserved		

Register 4-163: SPI Module GPIO Mode Data/Direction Register (SP04R: Index 10h, Offset 310h)

Bit	Bit Definition	Bit Value	Value Definition
2:0	R/W. Data Bits When the SPI Module is programmed to operate in GPIO Mode, these three bits are used as data bits. The bits [11:6] are associated with the following pins on the SPI interface. In Test 1 mode bits [1:0] are used as counter out. SPIMGPIO [0] = SCK, GPIO51 SPIMGPIO [1] = MOSI, GPIO52, TIME_GAP 16 bits Counter out (always 0) SPIMGPIO [2] = MISO, GPIO53, CLOCK DIVIDER 8bits Counter out (always 0)		

Register 4-163: SPI Module GPIO Mode Data/Direction Register (SP04R: Index 10h, Offset 310h)

Bit	Bit Definition	Bit Value	Value Definition
3	R/W. Data Bits When the LED Module is programmed to operate in GPIO Mode, these this bit is used as data bit. These bits SPIMGPIO [5:4] are associated with the following pin on the LED interface. And in Test 1 mode this bit is used as counter out. SPIMGPIO[3] = SS, LEDOUT, GPIO50, CLOCK DIVIDER 20 bits Counter out		
5:4	R/W. GPIO50/SS Control. These bits control GPIO50/SS pin when it is used as general purpose input/output	00	Input disabled, Output disabled
		01	Input disabled, Output enabled
		10	Input enabled, Output disabled
		11	Input enabled, Output enabled
7:6	R/W. GPIO51/SCK Control. These bits control GPIO51/SCK pin when it is used as general purpose input/output	00	Input disabled, Output disabled
		01	Input disabled, Output enabled
		10	Input enabled, Output disabled
		11	Input enabled, Output enabled
9:8	R/W. GPIO52/MOSI Control. These bits control GPIO52/MOSI pin when it is used as general purpose input/output	00	Input disabled, Output disabled
		01	Input disabled, Output enabled
		10	Input enabled, Output disabled
		11	Input enabled, Output enabled
11:10	R/W. GPIO53/MISO Control. These bits control GPIO53/MISO pin when it is used as general purpose input/output	00	Input disabled, Output disabled
		01	Input disabled, Output enabled
		10	Input enabled, Output disabled
		11	Input enabled, Output enabled
15:12	R/W. Pull Up Resister When reset goes low the pull up resisters are active. When reset goes high, the pads begins normal operation SPIMGPIO [12] = GPIO50PUE, 0:Active, 1:Inactive SPIMGPIO [13] = GPIO51PUE, 0:Active, 1:Inactive SPIMGPIO [14] = GPIO52PUE, 0:Active, 1:Inactive SPIMGPIO [15] = GPIO53PUE, 0:Active, 1:Inactive		
16	R/W. Data Bits When the GPIO50 pin is programmed to operate in LED out Mode, this bit is used as GPIO54 data bit. These bits SPIMGPIO [19:18] are associated with the following pin on the GPIO interface. SPIMGPIO[16] = GPIO54, LEDOUT		
17	R/W. Data Bits This bit is used as GPIO55 data bit. These bits SPIMGPIO [21:20] are associated with the following pin on the GPIO interface. SPIMGPIO[16] = GPIO55		

Register 4-163: SPI Module GPIO Mode Data/Direction Register (SP04R: Index 10h, Offset 310h)

Bit	Bit Definition	Bit Value	Value Definition
19:18	R/W. GPIO54 Control. These bits control GPIO54 pin when it is used as general purpose input/output	00	Input disabled, Output disabled
		01	Input disabled, Output enabled
		10	Input enabled, Output disabled
		11	Input enabled, Output enabled
21:20	R/W. GPIO55 Control. These bits control GPIO55 pin when it is used as general purpose input/output	00	Input disabled, Output disabled
		01	Input disabled, Output enabled
		10	Input enabled, Output disabled
		11	Input enabled, Output enabled
22	R/W. OSC clock select	0	Select osc clock
		1	Select bus clock
31:23	Reserved and will return a zero when read.		

Register 4-164: SPI Module Data Count Register (SP05R: Index 14h, Offset 314h)

Bit	Bit Definition	Bit Value	Value Definition
6:0	R/W. Data Count Value In case SPIMCR [31] is set and bit [7] of this register is zero, the SPI Module, when enabled, transfers the required number of data words mentioned in the data count register and sets the SPIMSR [0] to indicate completion of data transfer. In case SPIMCR [31] is set and bit [7] of this register is set with count value equal to 0, the SPI module, when enabled, transfers the data continuously until the software writes a value 0 into bit 7 of this register with a count value equal to 0. After completing the data transfer, SPI Transfer complete bit SPIMSR [0] is set.		
7	R/W. Continuous/Fixed Transfer Mode bit This bit is reset on power-on. This bit has meaning only when SPIMCR [31] is set.	0	Fixed Transfer Mode – Transfer the required number of words mentioned in bit [6:0] of this register and stops.
		1	Continuous Transfer Mode – Continuously transfer data. It is mandatory to write a value equal to 0 in the data count field of this register while setting this bit. Software can abort or stop by writing a value of zero into this bit and also a value of 0 into the Data Count field.
31:8	Reserved		

Register 4-165: SPI Module FIFO Threshold Register (SP06R: Index 18h, Offset 318h)

Bit	Bit Definition	Bit Value	Value Definition
6:0	R/W. Transmit FIFO Threshold Value The host programs the required threshold. Bits SPIMCR [10] and SPIMCR [21] are not masked and the FIFO threshold equals the value programmed in this register.	0000000	Transmit FIFO is Full
		0000001	1 location available.
		0000010	2 locations available.
		0000011	3 locations available.
		0000100	4 locations available.
		0000101	5 locations available.
		0000110	6 locations available.
		0000111	7 location available.
		0001000	8 locations available.
		0001001	9 locations available.
		0001010	10 locations available.
		0001011	11 locations available.
		0001100	12 locations available
		0001101	13 locations available.
		0001110	14 locations available.
		0001111	15 locations available.
		0010000	16 locations available
		0010001	17 location available.
		0010010	18 locations available.
		0010011	19 locations available.
		0010100	20 locations available.
		0010101	21 locations available.
		0010110	22 locations available.
		0010111	23 location available.
		0011000	24 locations available.
		0011001	25 locations available.
		0011010	26 locations available.
		0011011	27 locations available.
		0011100	28 locations available
		0011101	29 locations available.
		0011110	30 locations available.
		0011111	31 locations available.
		0100000	32 locations available. (Transmit FIFO Empty – for 16-bit mode of SPI Operation)

Register 4-165: SPI Module FIFO Threshold Register (SP06R: Index 18h, Offset 318h)

Bit	Bit Definition	Bit Value	Value Definition
6:0	R/W. Transmit FIFO Threshold Value The host programs the required threshold. Bits SPIMCR [10] and SPIMCR [21] are not masked and the FIFO threshold equals the value programmed in this register. ***Note:*** *A read of SP06R will return a 6 bit value which indicates the number of locations available in the transmit FIFO.* *8 Bit SPI Configuration:* *The Value returned will be in the range of 0000000 to 0111111, a value of 1000000 indicating the FIFO is empty.* *16 Bit SPI Configuration:* *The Value returned will be in the range of 000000 to 011111, a value of 100000 indicating the FIFO is empty.*	0100001	33 location available.
		0100010	34 locations available.
		0100011	35 locations available.
		0100100	36 locations available.
		0100101	37 locations available.
		0100110	38 locations available.
		0100111	39 location available.
		0101000	40 locations available.
		0101001	41 locations available.
		0101010	42 locations available.
		0101011	43 locations available.
		0101100	44 locations available
		0101101	45 locations available.
		0101110	46 locations available.
		0101111	47 locations available.
		0110000	48 locations available
		0110001	49 location available.
		0110010	50 locations available.
		0110011	51 locations available.
		0110100	52 locations available.
		0110101	53 locations available.
		0110110	54 locations available.
		0110111	55 location available.
		0111000	56 locations available.
		0111001	57 locations available.
		0111010	58 locations available.
		0111011	59 locations available.
		0111100	60 locations available
		0111101	61 locations available.
		0111110	62 locations available.
		0111111	63 locations available.
		1000000	Transmit FIFO is empty. (For 8-bit mode of SPI operation)
7	Reserved		

Register 4-165: SPI Module FIFO Threshold Register (SP06R: Index 18h, Offset 318h)

Bit	Bit Definition	Bit Value	Value Definition
14:8	R/W. Receive FIFO Threshold. The host programs the required threshold. Bit SPIMCR [10] and bit SPIMCR [25] are not masked and the FIFO threshold equals to the value programmed in this register, the SPIMSR [6] is set to 1.	0000000	Receive FIFO is Full
		0000001	1 location available.
		0000010	2 locations available.
		0000011	3 locations available.
		0000100	4 locations available.
		0000101	5 locations available.
		0000110	6 locations available.
		0000111	7 location available.
		0001000	8 locations available.
		0001001	9 locations available.
		0001010	10 locations available.
		0001011	11 locations available.
		0001100	12 locations available
		0001101	13 locations available.
		0001110	14 locations available.
		0001111	15 locations available.
		0010000	16 locations available
		0010001	17 location available.
		0010010	18 locations available.
		0010011	19 locations available.
		0010100	20 locations available.
		0010101	21 locations available.
		0010110	22 locations available.
		0010111	23 location available.
		0011000	24 locations available.
		0011001	25 locations available.
		0011010	26 locations available.
		0011011	27 locations available.
		0011100	28 locations available
		0011101	29 locations available.
		0011110	30 locations available.
		0011111	31 locations available.
		0100000	32 locations available. (Receive FIFO Empty – for 16-bit mode of SPI Operation)

Descriptions of Bits 14:8 are continued on the next page.

Register 4-165: SPI Module FIFO Threshold Register (SP06R: Index 18h, Offset 318h)

Bit	Bit Definition	Bit Value	Value Definition
14:8	R/W. Receive FIFO Threshold. The host programs the required threshold.Bit SPIMCR [10] and bit SPIMCR [25] are not masked and the FIFO threshold is equal to the value programmed in this register, The SPIMSR [6] is set to 1.	0100001	33 location available.
		0100010	34 locations available.
		0100011	35 locations available.
		0100100	36 locations available.
		0100101	37 locations available.
		0100110	38 locations available.
		0100111	39 location available.
		0101000	40 locations available.
		0101001	41 locations available.
		0101010	42 locations available.
		0101011	43 locations available.
		0101100	44 locations available
		0101101	45 locations available.
		0101110	46 locations available.
		0101111	47 locations available.
		0110000	48 locations available
		0110001	49 location available.
		0110010	50 locations available.
		0110011	51 locations available.
		0110100	52 locations available.
		0110101	53 locations available.
		0110110	54 locations available.
		0110111	55 location available.
		0111000	56 locations available.
		0111001	57 locations available.
		0111010	58 locations available.
		0111011	59 locations available.
		0111100	60 locations available
		0111101	61 locations available.
		0111110	62 locations available.
		0111111	63 locations available.
		1000000	Receive FIFO is empty. (For 8-bit mode of SPI Operation)
31:15	Reserved		

Register 4-166: LED Control Register (SP07R: Index 1Ch, Offset 31Ch) (MQ-1132 only)

Bit	Bit Definition	Bit Value	Value Definition
1:0	LED Mode Enable Bits. These two bits are used to program the mode of operation of the LED Module. On power on, the LED Pin LED come up as output. A value of 01 implies, the mode of operation of the LED Module is in LED mode. A value of 10, which is test mode 2, some of the counters internal to the SPI Module logic can be accessed directly to provide assistance in increasing the fault coverage. (Factory test mode only)	00	GPIO Mode is enabled.
		01	LED Mode is enabled.
		10	Test mode 2 enabled.
		11	Reserved
3:2	Reserved		
7:4	LED1 Clock Divider – First Level pre-divider Logic The SCK Clock is derived off either the oscillator clock or the bus clock. The clock output is pre-divided based on these bits to generate a LED1CLK.	0000	Divided by 1.
		0001	Divided by 2.
		0010	Divided by 3.
		0011	Divided by 4.
		0100	Divided by 5.
		0101	Divided by 6.
		0110	Divided by 7.
		0111	Divided by 8.
		1000	Divided by 9.
		1001	Divided by 10.
		1010	Divided by 11.
		1011	Divided by 12.
		1100	Divided by 13.
		1101	Divided by 14.
		1110	Divided by 15.
		1111	Divided by 16.
11:8	LED2 Clock Divider – Second Level pre-divider Logic The LED1CLK Clock is derived off either the oscillator clock or the bus clock. The clock output is pre-divided based on these bits to generate a LED2CLK.	0000	Divided by 1.
		0001	Divided by 2.
		0010	Divided by 3.
		0011	Divided by 4.
		0100	Divided by 5.
		0101	Divided by 6.
		0110	Divided by 7.
		0111	Divided by 8.
		1000	Divided by 9.
		1001	Divided by 10.
		1010	Divided by 11.
		1011	Divided by 12.
		1100	Divided by 13.
		1101	Divided by 14.
		1110	Divided by 15.
		1111	Divided by 16.

Register 4-166: LED Control Register (SP07R: Index 1Ch, Offset 31Ch) (MQ-1132 only)

Bit	Bit Definition	Bit Value	Value Definition
15:12	LED3 Clock Divider – Third Level pre-divider Logic The LED2 Clock is derived off either the oscillator clock or the bus clock. The clock output is pre-divided based on these bits to generate a LED3CLK.	0000	Divided by 1.
		0001	Divided by 2.
		0010	Divided by 3.
		0011	Divided by 4.
		0100	Divided by 5.
		0101	Divided by 6.
		0110	Divided by 7.
		0111	Divided by 8.
		1000	Divided by 9.
		1001	Divided by 10.
		1010	Divided by 11.
		1011	Divided by 12.
		1100	Divided by 13.
		1101	Divided by 14.
		1110	Divided by 15.
		1111	Divided by 16.
19:16	LED4 Clock Divider – Forth Level pre-divider Logic The LED3CLK Clock is derived off either the oscillator clock or the bus clock. The clock output is pre-divided based on these bits to generate a LED4CLK.	0000	Divided by 1.
		0001	Divided by 2.
		0010	Divided by 3.
		0011	Divided by 4.
		0100	Divided by 5.
		0101	Divided by 6.
		0110	Divided by 7.
		0111	Divided by 8.
		1000	Divided by 9.
		1001	Divided by 10.
		1010	Divided by 11.
		1011	Divided by 12.
		1100	Divided by 13.
		1101	Divided by 14.
		1110	Divided by 15.
		1111	Divided by 16.
23:20	LED5 Clock Divider – Fifth Level pre-divider Logic The LED4CLK Clock is derived off either the oscillator clock or the bus clock. The clock output is pre-divided based on these bits to generate a LED5CLK.	0000	Divided by 1.
		0001	Divided by 2.
		0010	Divided by 3.
		0011	Divided by 4.
		0100	Divided by 5.
		0101	Divided by 6.
		0110	Divided by 7.
		0111	Divided by 8.
		1000	Divided by 9.
		1001	Divided by 10.
		1010	Divided by 11.
		1011	Divided by 12.
		1100	Divided by 13.
		1101	Divided by 14.
		1110	Divided by 15.
		1111	Divided by 16.

Register 4-166: LED Control Register (SP07R: Index 1Ch, Offset 31Ch) (MQ-1132 only)

Bit	Bit Definition	Bit Value	Value Definition
27:24	LED6 Clock Divider – First Level pre-divider Logic The SCK Clock is derived off either the oscillator clock or the bus clock. The clock output is pre-divided based on these bits to generate a PDCLK.	0000	Divided by 1.
		0001	Divided by 2.
		0010	Divided by 3.
		0011	Divided by 4.
		0100	Divided by 5.
		0101	Divided by 6.
		0110	Divided by 7.
		0111	Divided by 8.
		1000	Divided by 9.
		1001	Divided by 10.
		1010	Divided by 11.
		1011	Divided by 12.
		1100	Divided by 13.
		1101	Divided by 14.
		1110	Divided by 15.
		1111	Divided by 16.
31:28	LED7 Clock Divider – First Level pre-divider Logic Clock Divider – Second Level post-divider logic The Timer counts down from the maximum value based on the clock derived from the oscillator clock or the Bus Clock based on the setting of bit SP04R [22]. This clock is further divided based on the setting of these bits.	0000	Divided by 1.
		0001	Divided by 2.
		0010	Divided by 3.
		0011	Divided by 4.
		0100	Divided by 5.
		0101	Divided by 6.
		0110	Divided by 7.
		0111	Divided by 8.
		1000	Divided by 9.
		1001	Divided by 10.
		1010	Divided by 11.
		1011	Divided by 12.
		1100	Divided by 13.
		1101	Divided by 14.
		1110	Divided by 15.
		1111	Divided by 16.

Register 4-167: Blue GPIO Mode Data/Direction Register (SP08R: Index 20h, Offset 320h) (MQ-1132 only)

Bit	Bit Definition	Bit Value	Value Definition
6:0	R/W. Data Bits These bits are used as data bits. Bits BLUMGPR [21:8] are associated with the following pin on the GPIO interface. BLUMGPR [0] = GPIO60 BLUMGPR [1] = GPIO61 BLUMGPR [2] = GPIO62 BLUMGPR [3] = GPIO63 BLUMGPR [4] = GPIO64 BLUMGPR [5] = GPIO65 BLUMGPR [6] = GPIO66		
7	Reserved	0	
9:8	R/W. GPIO60 Control. These bits control GPIO60 pin when it is used as general purpose input/output	00	Input disabled, Output disabled
		01	Input disabled, Output enabled
		10	Input enabled, Output disabled
		11	Input enabled, Output enabled

Register 4-167: Blue GPIO Mode Data/Direction Register (SP08R: Index 20h, Offset 320h) (MQ-1132 only)

Bit	Bit Definition	Bit Value	Value Definition
11:10	R/W. GPIO61 Control. These bits control GPIO61 pin when it is used as general purpose input/output	00	Input disabled, Output disabled
		01	Input disabled, Output enabled
		10	Input enabled, Output disabled
		11	Input enabled, Output enabled
13:12	R/W. GPIO62 Control. These bits control GPIO62 pin when it is used as general purpose input/output	00	Input disabled, Output disabled
		01	Input disabled, Output enabled
		10	Input enabled, Output disabled
		11	Input enabled, Output enabled
15:14	R/W. GPIO63 Control. These bits control GPIO63 pin when it is used as general purpose input/output	00	Input disabled, Output disabled
		01	Input disabled, Output enabled
		10	Input enabled, Output disabled
		11	Input enabled, Output enabled
17:16	R/W. GPIO64 Control. These bits control GPIO64 pin when it is used as general purpose input/output	00	Input disabled, Output disabled
		01	Input disabled, Output enabled
		10	Input enabled, Output disabled
		11	Input enabled, Output enabled
19:18	R/W. GPIO65 Control. These bits control GPIO65 pin when it is used as general purpose input/output	00	Input disabled, Output disabled
		01	Input disabled, Output enabled
		10	Input enabled, Output disabled
		11	Input enabled, Output enabled
21:20	R/W. GPIO66 Control. These bits control GPIO66 pin when it is used as general purpose input/output	00	Input disabled, Output disabled
		01	Input disabled, Output enabled
		10	Input enabled, Output disabled
		11	Input enabled, Output enabled
31:22	Reserved		

4.14.3. Details of the Data Transfer Formats

As discussed earlier, the SPI Module provides the flexibility to have various settings for the Clock Phase and the Clock Polarity while Transmitting or Receiving the data to or from an external peripheral respectively. The bits SPIMCR [5] and SPIMCR [6] correspond to the Clock Polarity and Clock Phase setting respectively. The clock phase control bit SPIMCR [6] selects one of the possible two transfer formats that affect the timings of the data transfer. It is important to note that the Clock Phase and the Clock Polarity should be the same for the Master as well as the Slave device. Based on the system requirements, the phase and polarity may be changed between transfers to accommodate a master device to communicate with different slave devices with different timing requirements. Adequate flexibility has been provided in this SPI Module design to communicate with different types of Master-Slave communication timing requirements. The details of the data transfer are as follows:

CPHA = 0 Transfer Format

The waveform shown in Figure 4-6, CPHA = 0 Transfer Format, explains the behavior of the SCK Signal, MOSI and MISO Signals and the expected generation of the Slave selects using one of the GPIOs when the SPI Module is programmed to operate in Master Mode and the contents of SPIMCR[6] is equal to 0.

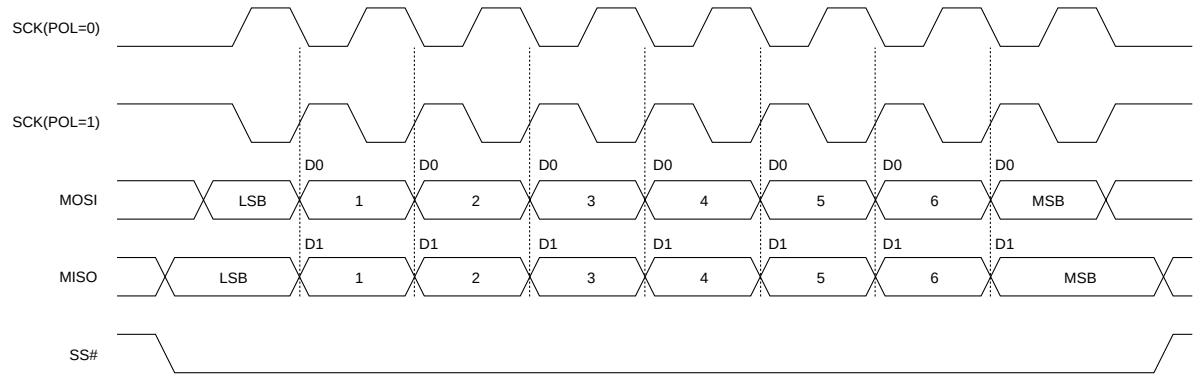


Figure 4-6. CPHA = 0 Transfer Format

Figure 4-6, CPHA = 0 Transfer Format, illustrates a SPI Data Transfer of 8-bit transfer size. The above diagram can correspond to either a master or a slave and can be inferred as timing waveforms associated with master or slave since the two are directly connected with the above signals. In case the SPI Module is programmed to operate in Master Mode, the SPI module drives the SCK Clock Signal. The inactive level of the clock when the SPIMCR[5] is programmed to 0 is low and the inactive level of the clock when the SPIMCR[5] is programmed to 1 is high. Based on the above waveform, it is clear that for the CPHA = 0 Transfer Format, the SCK Signal is inactive for the first half of the first SCK cycle. The SCK signal remains inactive for the first half of the first SCK cycle. Data is latched on the first and each subsequent out-clock edge, and the SPI shift register is left-shifted on the second and subsequent even-clock edges.

A write operation to the SPIMDR Register initiates the transfer shown above. For the slave device that is connected to the SPI master, which, in this case is the MQ-1132 chip (master), the falling edge of SS# signal indicates the start of a transfer. For the above waveform, software programmed the Serial Data Ordering Bit SPIMCR[3] to a value equal to 0, which implies the LSB bit of an 8-bit data is transferred first. The slave samples the transmitted data and the master samples the received data at the first and each succeeding odd clock edge. The master module generates the LSB data with adequate setup time before the first clock edge. The master drives the subsequent bits off of the second and successive even clock edges. For the CPHA = 0 Transfer Format, the Slave Select signal generated by the MQ-1132 using SS# pin asserted and de-asserted between each data transfer.

4.14.4. CPHA = 1 Transfer Format

The waveform shown in Figure 4-7, CPHA = 1 Transfer Format, explains the behavior of the SCK Signal, MOSI and MISO Signals and the expected generation of the Slave selects using one of the GPIOs when the SPI Module is programmed to operate in Master Mode and the contents of SPIMCR[6] is equal to 1.

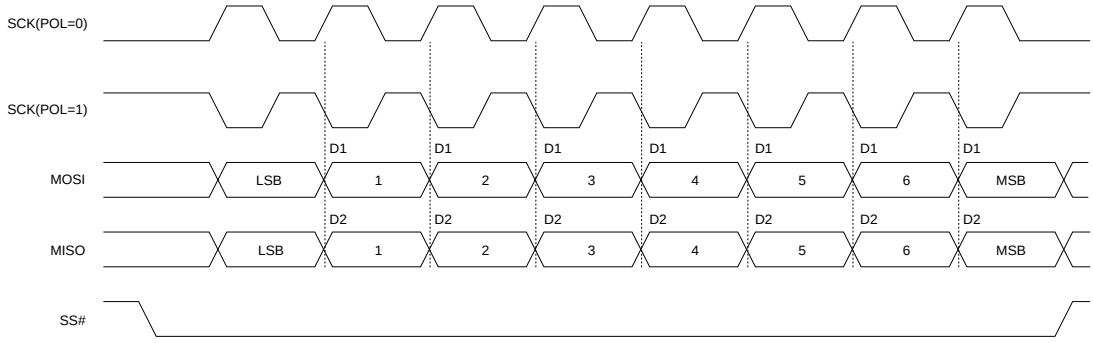


Figure 4-7. CPHA = 1 Transfer Format

Figure 4-7, CPHA = 1 Transfer Format, illustrates a SPI Data Transfer of 8-bit transfer size. This can correspond to either a master or a slave and can be inferred as timing waveforms associated with master or slave since the two are directly connected with the above signals. In case the SPI Module is programmed to operate in Master Mode, the SPI module drives the SCK clock signal. The inactive level of the clock when the SPIMCR[5] is programmed to 0 is low and the inactive level of the clock when the SPIMCR[5] is programmed to 1 is high. Based on the above waveform, it is clear that for the CPHA = 1 Transfer Format, the SCK Signal is inactive for the last half of the eighth SCK cycle. For a slave, the first edge of SCK indicates the start of a transfer. The SPI is left-shifted on the first and each subsequent odd-clock edge, and data is latched on the second and subsequent even-clock edges.

A write operation to the SPIMDR Register initiates the transfer shown above. For the slave device that is connected to the SPI master, which, in this case is the MQ-1132 (master), the first edge of SCK indicates the start of a transfer. For the above waveform, software programmed the Serial Data Ordering Bit SPIMCR[3] to a value equal to 0, which implies the LSB bit of an 8-bit data is transferred first. The slave samples the transmitted data and the master samples the received data at the second and each succeeding even clock edge. The master drives the LSB and subsequent bits off of the first and successive odd clock edges.

- For the CPHA = 0 Transfer Format, the Slave Select signal generated by the MQ-1132, on the SS#, must be asserted and de-asserted between each data transfer.
- For CPHA = 1 Transfer Format, the Slave Select signal SS# may remain at its active low level between each data transfer.

Figure 4-7 illustrates that the last edge associated with the SCK signal occurs in the middle of the MSB bit. The only way the slave knows about the completion of a data transfer is by keeping track of the data count of the number of bits sampled and comparing it with the transfer size.

Normally, the CPHA = 1 type of Transfer Format is used in systems having a single fixed master and only one slave that needs to drive the MISO data line. With an assumption that the Fault Mode detection is disabled, in case the MQ-1132 operates in Master Mode and is programmed to transfer data with CPHA = 1 type of data transfer, it can communicate with the slave device with only three pins.

4.14.5. Data Transfer – in Progress and Completion

Based on the previous discussion, the following is the inference with respect to the starting of a data transfer and completion of a data transfer.

4.14.6. Master Mode

Program these bits: SP00R bit[10] and SP00R bit[19]. The data transfer begins when the data is written into the SPIMDR register. The data transfer is complete when SPIMSR [0] is set. The host software has to write a 1 into this bit to clear.

4.14.7. Slave Mode

For a CPHA = 0 type of transfer format, the data transfer begins when the Slave Select Signal is asserted and ends when it is de-asserted.

For a CPHA = 1 type of transfer format, the data transfer begins at the first SCK clock edge and ends when the SPIMSR [0] is set.

4.14.8. Fault Condition Detection

The fault condition is detected only when the slave select pin which remains as input when the SPI module internal to the MQ-1132 is configured as a master and the fault detection is enabled, is asserted before a transfer begins or while the transfer is in progress. In such a situation, the SCK pin and the MOSI pins are tri-stated to avoid bus contention.

4.15 Synchronous Serial Channel (I^2S) (MQ-1132 only)

The MQ-1132 supports a full-duplex synchronous serial channel (I^2S) to interface to an external audio or modem codec chip in either master and slave mode.

The I^2S supports 5 different data formats for serial transmit, and receive. Both 16-bit and 8-bit data widths are supported. Formats that support stereo can be transmitted, or received, in mono mode. In mono mode transmit uses the same transmit FIFO entry for transmitting both right, and left. Mono mode receive uses a register bit to select if right, or left, data should be written to the receive FIFO.

Transmit FIFO data can be supplied by direct host writes to register SS12R, or through a DMA scheme which transfers data from the MQ-1132 embedded memory to the I^2S transmit fifo. This DMA scheme supports continuous data transfer through a ping-pong memory buffering scheme. Where the host can be re-initializing one buffer while the DMA controller is using the other buffer to supply data to the transmit fifo. Data is retrieved from the receive fifo by performing a host reads of register SS12R.

The source of I^2S root clock can be taken from the SRCLK pin, oscillator input, or the bus clock. The oscillator input is usually set to 48 MHz, because this is the frequency required by the USB interface. Bus clock varies in frequency depending on which processor is interfaced to the MQ-1132. The I^2S module contains a three stage clock divider. The first stage can be used to divide down the I^2S root clock to generate a master clock, SMCLK. The second stage can be used to divide down the master clock, SMCLK, to generate a bit clock, SCLK. And the third stage can be used to divide down the bit clock, SCLK, to generate a Frame Synchronization clock, FSYNC. These three clocks are described in more detail on page 217.

- SMCLK – this is *master* clock for external device attached to this interface. This clock can be internally derived from the root clock. The maximum frequency of this clock is 24.576 MHz for audio codec and 36.864 MHz for modem codec. This clock is not always needed because some codec can generate its master clock using a built-in clock oscillator. In the case where external codec generates a master clock output, it is possible to use the codec's master clock as input to the I^2S module (to SRCLK pin) and use it as *root* clock in which case no internal clocks are needed.
- SCLK – this is the clock for serial data transmission and reception. This is basically the *oversampling* frequency for the audio or modem signal. This clock is generated from the master clock. The maximum frequency for this clock is 12.288 MHz for audio codec and 18.432 MHz for modem codec. This clock can be generated internally in the I^2S module or externally by the codec.
- FSYNC – this is the clock for frame synchronization and is used to indicate the beginning of data transmission. This is also *sampling* frequency (Fs) for the audio or modem signal. For audio purpose maximum frequency is 48 KHz, and for V.34 and 56 Kbps modem the maximum frequency is 16 KHz.

I^2S has six interface pins: SRCLK, SMCLK, SCLK, FSYNC, SIN, and SOUT.

4.15.1. Register Definitions

Table 4-16 specifies the index, offset and reset values for the I^2S registers.

TABLE 4-16: I^2S Register Index and Reset Values

Register	Index	Offset	Reset Value	See Description
SS00R	00h	280h	0000-0000h	*Register 4-168 on page 218*
SS01R	04h	284h	0000-0000h	*Register 4-169 on page 220*
SS04R	10h	290h	xxxx-xxx0h	*Register 4-170 on page 223*
SS08R	20h	2A0h	xxxx-xx00h	*Register 4-171 on page 224*
SS09R	24h	2A4h	xxxx-xx00h	*Register 4-172 on page 224*
SS0AR	28h	2A8h	xxxx-xx00h	*Register 4-173 on page 225*
SS0BR	2Ch	2ACh	xxxx-xx00h	*Register 4-174 on page 225*
SS0CR	30h	2B0h	xxxx-xxxxh	*Register 4-175 on page 225*
SS0DR	34h	2B4h	xxxx-xxxxh	*Register 4-176 on page 226*
SS10R	40h	2C0h	0000-0000h	*Register 4-177 on page 226*
SS11R	44h	2C4h	0000-0000h	*Register 4-178 on page 230*
SS12R	48h	2C8h		*Register 4-179 on page 232*
SS13R	4Ch	2CCh	0000-0000h	*Register 4-180 on page 232*
SS14R	50h	2D0h	xxxx-xxxxh	*Register 4-181 on page 233*
SS15R	54h	2D4h	xxxx-xxxxh	*Register 4-182 on page 233*

The clock divide and synchronization generation register (see *Register 4-168*) sets clock divide values and parameters for generating master clock, bit clock and Frame Sync. The clock divider flip-flops are automatically reset when this register is written. This is done to insure a clean start-up of the clock divider.

Register 4-168: Clock Divide and Synchronization Generation Register (SS00R: Index 00h, Offset 280h)

Bit	Bit Definition	Bit Value	Value Definition
2:0	I^2S Root Clock Source This field is used to select the source for root clock.	000	SRCLK pin is used to input root clock for I^2S. GPIO40 (SRCLK) pin must be configured in input mode.
		001	Reserved.
		010	Reserved.
		011	Reserved.
		100	SRCLK source is the oscillator input.
		101	SRCLK source is Bus Clock
		110	Reserved.
		111	Reserved.
3	FSYNC Signal Direction.	0	FSYNC signal is input, and is used for internal frame synchronization. The clock divide logic used to generate the internal FSYNC is powered down. GPIO43 (FSYNC) pin must be configured in input mode.
		1	FSYNC signal is output. GPIO43 (FSYNC) pin must be configured to output FSYNC signal.
4	SCLK Signal Direction.	0	SCLK signal is input. GPIO42 (SCLK) pin must be configured in input mode.
		1	SCLK signal is output. GPIO42 (SCLK) pin must be configured to output SCLK signal.
6:5	SMCLK Pre-divider (MP2) Parameter This parameter and bits 15-8 are used to generate SMCLK from the root clock. When SS00R[15:12] = 1111, SMCLK will be driven with the value stored in SS00R[5] and SMCLK logic will be powered down. See description of bits 15-12.	00	MP2 = 2.
		01	MP2 = 3.
		10	MP2 = 2.5
		11	Reserved.
7	Serial data Delay	0	SOUT data is not delayed so that first bit of data (MSB) comes out immediately following a FSYNC edge. Likewise FSYNC edge and the first bit (MSB) of SIN data is sampled on the same SCLK edge.
		1	SOUT output data is delayed by 1 SCLK cycle so that first output data (MSB) comes out one SCLK cycle following a FSYNC edge. Likewise the first bit (MSB) on SIN is sampled: one SCLK following a FSYNC edge.
11:8	SMCLK Pre-Divider (MP1) Parameter This parameter and bits 15-12 are used to generate SMCLK from the root clock. See description of bits 15-12.	0000	MP1 = 1.5.
		0001	MP1 = 2.
		0010	MP1 = 2.5.
		0011	MP1 = 3.5.
		0100	MP1 = 4.5.
		0101	MP1 = 5.5.
		0110	MP1 = 6.5.
		0111	MP1 = 4.25
		1000	MP1 = 7.5
		other	Reserved

Register 4-168: Clock Divide and Synchronization Generation Register (SS00R: Index 00h, Offset 280h)

Bit	Bit Definition	Bit Value	Value Definition
15:12	SMCLK Generation Control This parameter is used to generate internal SMCLK. The first pre-divider (MP1) is defined in bits 11-8, and the second (MP2) is defined in bits 6-5. This internal signal is output on SMCLK pin if SMCLK pad output is enabled and SMCLK is selected as its output (SS08R[1] =1, SS0AR[1] = 0, and SS0BR [1] = 0).	0000	SMCLK = root clock.
		0001	SMCLK = root clock / MP1.
		0010	SMCLK = root clock / MP1 / MP2.
		0011	SMCLK = root clock / MP1 / MP2/2.
		0100	SMCLK = root clock / MP1 / MP2/4.
		0101	SMCLK = root clock / MP1 / MP2/8.
		0110	SMCLK = root clock / MP1 / MP2/16.
		0111	SMCLK = root clock / MP1 / MP2/32.
		1000	SMCLK = root clock / MP1 / MP2/64.
		1001	SMCLK = root clock / MP1 / MP2/128.
		1111	SMCLK is driven with the value in SS00R[5]. SCLK and FSYNC will also be stopped if they are generated internally. SMCLK generation logic be powered down in this case.
		Other	Reserved.
17:16	SCLK Pre-Divider (SP) Parameter This parameter and bits 20-18 are used to generate SCLK from internal SMCLK clock when SCLK is programmed as output pin. Please see description of bits 20-18.	00	SP = 1.
		01	SP = 2.
		10	SP = 3.
		11	SP = 5.
20:18	SCLK Generation Control This parameter is used to generate SCLK from internal SMCLK clock when SCLK is programmed as output pin. The pre-divider (SP) is defined in bits 17-16.	000	SCLK = SMCLK / SP.
		001	SCLK = SMCLK / SP / 2.
		010	SCLK = SMCLK / SP / 4.
		011	SCLK = SMCLK / SP / 8.
		100	SCLK = SMCLK / SP / 16.
		101	SCLK = SMCLK / SP / 32.
		110	SCLK = SMCLK / SP / 64.
		111	Reserved
21	SCLK Polarity If SCLK signal is output then, this bit is used to optionally enable inversion of SCLK. If SCLK signal is input, this bit is used to indicate which edge of SCLK is used to latch data input or FSYNC input.	0	SCLK signal is not inverted so that data and FSYNC output is generated at rising edge of SCLK. Data and FSYNC input must be latched with falling edge of SCLK.
		1	SCLK signal is inverted so that data and FSYNC output is generated at falling edge of SCLK. Data and FSYNC input must be latched with rising edge of SCLK.
23:22	FSYNC Pre-Divider (FP) Parameter This parameter is used to generate FSYNC when FSYNC is programmed as output pin. Please see description of bits 26-24.	00	FP = 1.
		01	FP = 2.
		10	FP = 3.
		11	FP = 5.
26:24	FSYNC Generation Control This parameter is used to generate internal FSYNC when FSYNC is programmed as output pin. The pre-divider (FP) is defined in bits 23-22. FSYNC polarity is controlled by bit 27.	000	FSYNC = SCLK / FP / 4.
		001	FSYNC = SCLK / FP / 8.
		010	FSYNC = SCLK / FP / 16.
		011	FSYNC = SCLK / FP / 32.
		100	FSYNC = SCLK / FP / 64.
		101	FSYNC = SCLK / FP / 128.
		110	Reserved.
		111	FSYNC is driven with bit 23 if bit 27 is set low or driven with inverse of bit 23 if bit 27 is set high.

Register 4-168: Clock Divide and Synchronization Generation Register (SS00R: Index 00h, Offset 280h)

Bit	Bit Definition	Bit Value	Value Definition
27	FSYNC Polarity This bit effects how the logic levels on FSYNC are used to determine which edge is the active, and which is the inactive edge. It is effective regardless of whether FSYNC is input or output as specified by SS00R[3] above.	0	FSYNC signal is not inverted. In this case, falling edge of FSYNC is used to indicate the beginning of serial data transmission. So, falling edge of FSYNC is the active edge of FSYNC.
		1	FSYNC signal is inverted. In this case, rising edge of FSYNC is used to indicate the beginning of serial data transmission. So, rising edge of FSYNC is the active edge of FSYNC.
29:28	FSYNC Pulse Type	00	FSYNC signal has even duty cycle.
		01	FSYNC signal is one SCLK wide generated once per frame. If FSYNC is an output, internally this output pulse is generated such that its falling edge coincides with falling edge of internal FSYNC.
		10	FSYNC signal is one SCLK wide generated twice per frame. If FSYNC is an output, internally this output pulse is generated once at the rising edge and once at the falling edge of internal FSYNC.
		11	Drive the internal FSYNC low. If FSYNC is defined as output and the FSYNC Polarity bit (SS00R[27]) is set to non-inverted, the external FSYNC pad will also be driven low. If FSYNC polarity is set to inverting, the FSYNC pad will be driven high.
30	SCLK value when stopped This parameter is only effective when SCLK is output, and has been stopped by clearing SS04R[1].	0	SCLK will be held at a logic 0 value when stopped.
		1	SCLK will be held at a logic 1 value when stopped.
31	FSYNC value when stopped This parameter is only effective when FSYNC is output, and has been stopped by clearing SS04R[2].	0	FSYNC will be held at a logic 0 value when stopped.
		1	FSYNC will be held at a logic 1 value when stopped.

SS01R[15:0] are read/write bits, which are used for interrupt source enables. SS01R[31:16] returns interrupt status when read, and resets interrupting conditions for interrupt status bit positions when written with 1. Interrupt status bit position written with 0 will be left unchanged. See *Register 4-169*.

To allow for software polling; interrupt status bits will still be set when their interrupting condition occurs, even if their interrupt enable bit is cleared. They also can still be cleared, or left unchanged, by writing 1, or 0, respectively to their SS001R[31:16] bit position.

Register 4-169: Interrupt Control and Status Register (SS01R: Index 04h, Offset 284h)

Bit	Bit Definition	Bit Value	Value Definition
3:0	Reserved. Must be programmed to 0.		
4	FSYNC Stopped Interrupt Enable This is effective when FSYNC is being generated internally.	0	Interrupt is not generated when the FSYNC stop operation, requested by clearing SS04R[2], has been completed.
		1	Interrupt is generated when the FSYNC stop operation, requested by clearing SS04R[2], has completed.
5	Reserved. Must be programmed to 0.		
6	Codec Receive FIFO Interrupt Enable This is effective when SS11R[0]=1 (Codec Receiver Enabled).	0	Interrupt is not generated when the Codec Receive fifo has at least as many entries in it as is programmed in the receive fifo threshold, SS11R[21:16].
		1	Interrupt is generated when the Codec Receive fifo has at least as many entries in it as is programmed in the receive fifo threshold, SS11R[21:16].

Register 4-169: Interrupt Control and Status Register (SS01R: Index 04h, Offset 284h)

Bit	Bit Definition	Bit Value	Value Definition
7	Codec Receive FIFO Overflow Interrupt Enable This is effective when SS11R[0]=1 (Codec Receiver Enabled).	0	Interrupt is not generated when Codec Receives fifo overflows.
		1	Interrupt is generated when Codec Receives fifo overflows.
8	Codec Transmit DMA Complete Interrupt Enable This is effective when SS10R[0]=1 (Codec Transmit Enabled) and SS10R[3] = 1 (Codec Transmit DMA Enabled).	0	Interrupt is not generated when Codec Transmit DMA has completed
		1	Interrupt is generated when the DMA transfer has completed. DMA transfer complete is signaled when the transfer count of the current buffer has expired and the next buffer is not enabled, or has its DMA finished status bit set. Buffer 1 is enabled by setting SS10R[4], buffer 2 is enabled by setting SS10R[5]. DMA finished status bit for buffer 1 is stored in SS10R[25], buffer 2 is stored in SS01R[26].
9	Codec Transmit Buffer 1 DMA Finished Interrupt Enable This is effective when SS10R[0]=1 (Codec Transmit Enabled), SS10R[3] = 1 (Codec Transmit DMA Enabled), and SS10R[4]=1 (Buffer 1 enabled).	0	Interrupt is not generated when the DMA from Buffer 1 has completed.
		1	Interrupt is generated when the DMA from Buffer 1 has completed. Buffer 1 DMA complete being signaled when the transfer count for buffer 1 has expired.
10	Codec Transmit Buffer 2 DMA Finished Interrupt Enable This is effective when SS10R[0]=1 (Codec Transmit Enabled), SS10R[3] = 1 (Codec Transmit DMA Enabled), and SS10R[5]=1 (Buffer 2 enabled).	0	Interrupt is not generated when the DMA from Buffer 2 has completed.
		1	Interrupt is generated when the DMA from Buffer 2 has completed. Buffer 2 DMA complete being signaled when the transfer count for buffer 2 has expired.
11	Codec Transmit FIFO Status Interrupt Enable. This interrupt should not be enabled when transmit is being operated in DMA mode.	0	An Interrupt will not be generated when the number of empty locations in the transmit fifo is equal to, or exceeds, the value programmed in SS10R[20:16].
		1	An Interrupt will be generated when the number of empty locations in the transmit fifo is equal to, or exceeds, the value programmed in SS10R[20:16].
12	Codec Transmit FIFO Out of Data Interrupt Enable Codec Transmit FIFO out of data interrupt should only be enabled when the transmit is operating in DMA mode. In non-DMA mode the logic can not distinguish a fifo out of data condition from a transmit complete.	0	Interrupt is not generated when Codec Transmit fifo runs out of data.
		1	Interrupt is generated when the Codec Transmit fifo runs out of data, before DMA has completed.
13	Codec Transmit Complete Interrupt Enable.	0	Interrupt is not generated when Codec Transmit is finished.
		1	Interrupt is generated when Codec Transmit is finished. In DMA mode transmit complete is signaled when the DMA complete status bit, SS01R[24], is set and the transmit fifo runs out of data. In non-DMA mode, transmit complete is signaled when the transmit fifo runs out of data. This may cause a false transmit complete signal if the host lets the transmit fifo run out of data before transmit is complete.
14	Reserved		
15	Frame Sync Interrupt Enable	0	Do not generate Interrupt when Frame Sync edge is detected.
		1	Interrupt when a Frame Sync, fsync, edge is detected. If SS04R[3] is set the interrupt is generated when the active (falling) edge of Fsync is detected. If SS04R[3] is clear inactive (rising) edge is used.
19:16	Reserved. Must be programmed to 0.		

Register 4-169: Interrupt Control and Status Register (SS01R: Index 04h, Offset 284h)

Bit	Bit Definition	Bit Value	Value Definition
20	FSYNC Stopped Status This status bit is set when the Frame Sync stop operation, requested by clearing SS04R[2], has completed. This status can be used to signal when it is safe to shut down the other clocks. Writing 1 to this bit will clear the status and its interrupt. This status bit, and its interrupt, are also cleared when SS04R[2] is set (FSYNC enabled).	0	No status.
		1	FSYNC is stopped.
21	Reserved. Must be programmed to 0.		
22	Codec Receive FIFO Status This is effective when SS11R[0]=1 (Codec Receiver Enable). This status bit and its interrupt will be cleared when the receive fifo level goes below its threshold.	0	Codec Receive fifo level is below its threshold.
		1	Codec Receive fifo level is at or above its threshold.
23	Codec Receive FIFO Overflow Status This bit is qualified with SS11R[0] (Codec Receiver Enable). Writing 1 to this bit will clear this status bit and its interrupt.	0	Codec Receive FIFO has not overflowed.
		1	Codec Receive FIFO overflow. Some of the data in the receive FIFO will get overwritten when an overflow occurs.
24	Codec Transmit DMA Complete Status This is effective when SS10R[0]=1 (Codec Transmit Enabled) and SS10R[3] = 1 (Codec Transmit DMA Enabled). Writing 1 to this bit will clear this status bit and its interrupt.	0	Transmit DMA has not completed.
		1	Transmit DMA has completed. See the description of SS01R[8]=1, for a description of how DMA Complete is signaled.
25	Codec Transmit Buffer 1 DMA Finished Status This is effective when SS10R[0]=1 (Codec Transmit Enabled), SS10R[3] = 1 (Codec Transmit DMA Enabled), and SS10R[4]=1 (Buffer 1 enabled). Writing 1 to this bit will clear this status bit and its interrupt.	0	DMA transfer from Buffer 1 is either active, has not started, or is not enabled (SS10R[4] = 0).
		1	DMA transfer from Buffer 1 has finished. This status must be cleared before the DMA will use buffer 1 again.
26	Codec Transmit Buffer 2 DMA Finished Status This is effective when SS10R[0]=1 (Codec Transmit Enabled), SS10R[3] = 1 (Codec Transmit DMA Enabled), and SS10R[5]=1 (Buffer 2 enabled). Writing 1 to this bit will clear this status bit and its interrupt.	0	DMA transfer from Buffer 2 is either active, has not started yet, or is not enabled (SS10R[5] = 0).
		1	DMA transfer from Buffer 2 has finished. This status must be cleared before the DMA will use buffer 2 again.
27	Codec Transmit FIFO Status This status bit, and its interrupt, will be cleared when the number of empty location in the transmit fifo goes below its threshold (SS10R[20:16]). This status bit, and its interrupt, should only be used when transmit DMA mode is not enabled (SS10R[3] = 0).	0	Codec Transmit fifo has less than the Transmit FIFO Threshold, SS10R[20:16], empty locations.
		1	Codec Transmit fifo has at least as many empty locations as is programmed in the transmit fifo threshold field, SS10R[20:16].
28	Codec Transmit FIFO out of data Status This status bit is only valid when DMA mode is enabled. In non-DMA mode the logic can not distinguish a fifo out of data condition from a transmit complete. Writing 1 to this bit will clear this status bit and its interrupt.	0	Codec Transmit fifo has not run out of data.
		1	Codec Transmit fifo ran out of data before transmit was complete. Logic will prevent the fifo under run by not popping the fifo when it outs of data, and transmitting zeros for the frame that didn't have data.

Register 4-169: Interrupt Control and Status Register (SS01R: Index 04h, Offset 284h)

Bit	Bit Definition	Bit Value	Value Definition
29	Codec Transmit Complete Status Writing 1 to this bit will clear this status bit and its interrupt.	0	Codec Transmit has not complete.
		1	Codec Transmit has finished. In DMA mode transmit complete is detected when the transmit FIFO runs out of data and the DMA complete status, SS01R[24], is set. In non-DMA mode Transmit complete is detected when the fifo runs out of data.
30	Reserved		
31	Frame Sync Status Writing 1 to this bit will clear this status bit and its interrupt.	0	The Frame Sync edge selected by SS04R[3] has not been detected.
		1	The Frame Sync edge selected by SS04R[3] has been detected.

Register 4-170: Clock Enable and FSYNC Edge Select Register (SS04R: Index 10h, Offset 290h)

Bit	Bit Definition	Bit Value	Value Definition
0	Enable Root Clock This bit should be used to stop root clock. When this bit is cleared, to avoid generating short pulses on root clock, logic will wait until root clock goes low before holding it low.	0	Root clock (the input to the clock divider) will stop. When stopped root clock will be held low.
		1	Root Clock is enabled.
1	Enable SCLK This parameter is only effective when SCLK signal is output. In order to start up SCLK cleanly, without generating short cycles, or glitching, SCLK control logic needs to have the internal bit clock running before SCLK enable bit is set. This can be accomplished by first doing a write to SS00R which sets the correct root clock source (SS00R [2:0]), root and master clock divide values (SS00R bits 20-8) with the Enable SCLK bit cleared. Waiting at least the equivalent time to one bit clock cycle, and the write to SS04R to enable SCLK.	0	SCLK is stopped. SCLK clock will be held at the value programmed in SS00R[30].
		1	SCLK is enabled.
2	Enable Frame Sync This parameter is only effective when FSYNC is output This bit should be used to stop frame FSYNC is output. When this bit is cleared, to void generating short pulses on FSYNC, logic will wait until FSYNC goes to its stop value (SS00R[31]) before holding it at this value. When this bit is set, to avoid generating short pulses on FSYNC, the logic will wait until the clock divider generated version of FSYNC goes to the value programmed in SS00R[31] before letting FSYNC start running.	0	FSYNC is stopped. FSYNC clock will be held at the value programmed in SS00R[31].
		1	FSYNC is enabled.
3	Frame Sync Status Edge Select This bit is used to select which edge of Frame Sync is used to set Frame Sync Status (SS01R[31].	0	Frame Sync Status (SS01R[31]) will be set when an inactive (rising) edge of Fsync has been detected.
		1	Frame Sync Status will be set when an active (falling) edge of Fsync has been detected.
31:4	Reserved		

Register 4-171: GPIO[45:40] Pin Output Control Register (SS08R: Index 20h, Offset 2A0h)

Bit	Bit Definition	Bit Value	Value Definition
0	GPIO40 (SRCLK) output control This bit controls output buffer of GPIO40(SRCLK) pin.	0	GPIO40 (SRCLK) output is disabled.
		1	GPIO40 (SRCLK) output is enabled.
1	GPIO41 (SMCLK) output control This bit controls output buffer of GPIO41(SMCLK) pin.	0	GPIO41 (SMCLK) output is disabled.
		1	GPIO41 (SMCLK) output is enabled.
2	GPIO42 (SCLK) output control This bit controls output buffer of GPIO42(SCLK) pin.	0	GPIO42 (SCLK) output is disabled.
		1	GPIO42 (SCLK) output is enabled.
3	GPIO43 (FSYNC) output control This bit controls output buffer of GPIO43(FSYNC) pin.	0	GPIO43 (FSYNC) output is disabled.
		1	GPIO43 (FSYNC) output is enabled.
4	GPIO44 (SIN) output control This bit controls output buffer of GPIO44 (SIN) pin.	0	GPIO44 (SIN) output is disabled.
		1	GPIO 44 (SIN) output is enabled.
5	GPIO45 (SOUT) output control This bit controls output buffer of GPIO45 (SOUT) pin.	0	GPIO45 (SOUT) output is disabled.
		1	GPIO 45 (SOUT) output is enabled.
31:6	Reserved		

Register 4-172: GPIO[45:40] Pin Input Control Register (SS09R: Index 24h, 2A4h)

Bit	Bit Definition	Bit Value	Value Definition
0	GPIO40 (SRCLK) input control This bit controls input buffer of GPIO40(SRCLK) pin.	0	GPIO40 (SRCLK) input is disabled.
		1	GPIO40 (SRCLK) input is enabled. Input data can be read from SS0DR[0].
1	GPIO41 (SMCLK) input control This bit controls input buffer of GPIO41(SMCLK) pin.	0	GPIO41 (SMCLK) input is disabled.
		1	GPIO41 (SMCLK) input is enabled. Input data can be read from SS0DR[1].
2	GPIO42 (SCLK) input control This bit controls input buffer of GPIO42(SCLK) pin.	0	GPIO42 (SCLK) input is disabled.
		1	GPIO42 (SCLK) input is enabled. Input data can be read from SS0DR[2].
3	GPIO43 (FSYNC) input control This bit controls input buffer of GPIO43(FSYNC) pin.	0	GPIO43 (FSYNC) input is disabled.
		1	GPIO43 (FSYNC) input is enabled. Input data can be read from SS0DR[3].
4	GPIO44 (SIN) input control This bit controls input buffer of GPIO44 (SIN) pin.	0	GPIO44 (SIN) input is disabled.
		1	GPIO 44 (SIN) input is enabled. Input data can be read from SS0DR[4].
5	GPIO45 (SOUT) input control This bit controls input buffer of GPIO45 (SOUT) pin.	0	GPIO45 (SOUT) input is disabled.
		1	GPIO 45 (SOUT) input is enabled. Input that can be read from SS0DR[5]
31:6	Reserved		

Register 4-173: GPIO[45:40] Pin Output Select 0 Register (SS0AR: Index 28h, Offset 2A8h)

Bit	Bit Definition	Bit Value	Value Definition
0	GPIO40 (SRCLK) input select 0 This bit and SS0BR[0] control output of GPIO40 (SRCLK) pin.	0	If SS0BR[0]=0, GPIO40 (SRCLK) pin outputs SRCLK signals. If SS0BR[0]=1, GPIO40 (SRCLK) pin outputs SS0CR[0].
		1	If SS0BR[0]=0, GPIO40 (SRCLK) pin is used for testing. If SS0BR[0]=1, GPIO40 (SRCLK) pin is used for testing.
1	GPIO41 (SMCLK) input select 0 This bit and SS0BR[1] control output of GPIO41 (SMCLK) pin.	0	If SS0BR[1]=0, GPIO41 (SMCLK) pin outputs SMCLK signals. If SS0BR[1]=1, GPIO41 (SMCLK) pin outputs SS0CR[1].
		1	If SS0BR[1]=0, GPIO41 (SMCLK) pin is used for testing. If SS0BR[1]=1, GPIO41 (SMCLK) pin is used for testing.
2	GPIO42 (SCLK) input select 0 This bit and SS0BR[2] control output of GPIO42 (SCLK) pin.	0	If SS0BR[2]=0, GPIO42 (SCLK) pin outputs SCLK signals. If SS0BR[2]=1, GPIO42 (SCLK) pin outputs SS0CR[2].
		1	If SS0BR[2]=0, GPIO42 (SCLK) pin is used for testing. If SS0BR[2]=1, GPIO42 (SCLK) pin is used for testing.
3	GPIO43 (FSYNC) input select 0 This bit and SS0BR[3] control output of GPIO43 (FSYNC) pin.	0	If SS0BR[3]=0, GPIO43 (FSYNC) pin outputs FSYNC signals. If SS0BR[3]=1, GPIO43 (FSYNC) pin outputs SS0CR[3].
		1	If SS0BR[3]=0, GPIO43 (FSYNC) pin is used for testing. If SS0BR[3]=1, GPIO43 (FSYNC) pin is used for testing.
4	GPIO44 (SIN) input select 0 This bit and SS0BR[4] control output of GPIO44 (SIN) pin.	0	If SS0BR[4]=0, GPIO44 (SIN) pin outputs SIN signals. If SS0BR[4]=1, GPIO44 (SIN) pin outputs SS0CR[4].
		1	If SS0BR[4]=0, GPIO44 (SIN) pin is used for testing. If SS0BR[4]=1, GPIO44 (SIN) pin is used for testing.
5	GPIO45 (SOUT) input select 0 This bit and SS0BR[5] control output of GPIO45 (SOUT) pin.	0	If SS0BR[5]=0, GPIO45 (SOUT) pin outputs SOUT signals. If SS0BR[5]=1, GPIO45 (SOUT) pin outputs SS0CR[5].
		1	If SS0BR[5]=0, GPIO45 (SOUT) pin is used for testing. If SS0BR[5]=1, GPIO45 (SOUT) pin is used for testing.
31:6	Reserved		

Register 4-174: GPIO[45:40] Pin Output Select 1 Register (SS0BR: Index 2Ch, 2ACh)

Bit	Bit Definition	Bit Value	Value Definition
5:0	GPIO[45:40] Pin Output Select 1		These bits and the corresponding bits in SS0AR control the output signals on GPIO[45:40] interface pins.
31:6	Reserved		

Register 4-175: GPIO[45:40] Pin Output Data Register (SS0CR: Index 30h, 2B0h)

Bit	Bit Definition	Bit Value	Value Definition
5:0	GPIO[45:40] Pin Output Data		These bits can be output on GPIO[45:40] interface pins when they are selected as output (see SS0AR).
31:6	Reserved		

Register 4-176: GPIO[45:40] Pin Input Data Register (SS0DR: Index 34h, 2B4h)

Bit	Bit Definition	Bit Value	Value Definition
5:0	GPIO[45:40] Pin Input Data		GPIO[45:40] interface pins can be read on these bits when the corresponding pin input buffer is enables (see SS09R).
31:6	Reserved		

Register 4-177 through *Register 4-182 on page 233*, provide Codec information.

Register 4-177: Codec Transmit Control Register (SS10R: Index 40h, Offset 2C0h)

Bit	Bit Definition	Bit Value	Value Definition
0	Transmit Enable	0	Transmitter is powered down.
		1	Transmitter is enabled.
1	This bit is used directly to enable the transmit bit clock. SS10R[1] should be held low when changing SS10R[0] from 0 to 1. This will makes sure the transmit logic is reset when the Transmit bit clock is first started.	0	Reset Tansmit FIFO and state machine, clear transmit bits (SS01R [29:24]) and abort transmit DMA if active.
		1	Normal Operation.
2	Transmit FIFO Logic Enable	0	If neither Transmit Enable or Transmit DMA Enable (SS10R[0] or SS10R[3]) are set, the Transmit FIFO logic will be powered down. With the FIFO logic powered down the FIFO status read from SS10R[29:24] may not be valid, and the FIFO can not be written to.
		1	Transmit FIFO logic will be powered up even if both Transmit Enable and Transmit DMA Enable (SS10R[0] and SS10R[3]) are disabled.
3	Codec Transmit DMA Enable This bit is qualified with SS10R[0] (I^2S) Codec Transmitter Enable).	0	Disabled
		1	Enable DMA to the transmit FIFO.
4	Codec Transmit DMA Buffer 1 Enable This bit is qualified with SS10R[3] (I^2S) Codec Transmitter DMA Enable).	0	Buffer 1 will not be used for DMA transfers.
		1	Buffer 1 enabled.
5	Codec Transmit DMA Buffer 2 Enable This bit is qualified with SS10R[3] (I^2S) Codec Transmitter DMA Enable).	0	Buffer 2 will not be used for DMA transfers.
		1	Buffer 2 enabled.
7:6	Reserved		
9:8	Transfer Width This field specifies the number of bits to be transmitted from each FIFO read.	00	8 bits, transmit bits 7-0.
		01	16 bits, transmit bits 15-0.
		10	Reserved.
		11	Reserved.
10	Transmit Mono Audio This bit is only effective when SS10R[14:12] is set to either 011, 100, or 101.	0	Stereo audio: data sent in the beginning of frame and data sent in the middle of frame come from two consecutive fifo locations.
		1	Mono audio: data sent in the middle of frame is a duplicate of data sent in the beginning of frame and both data words come from the same fifo location.
11	Reserved.		

Register 4-177: Codec Transmit Control Register (SS10R: Index 40h, Offset 2C0h)

Bit	Bit Definition	Bit Value	Value Definition
14:12	Serial Data Out Format This parameter specifies the serial data output format. In the below description the width of "word" is determined by the transfer width field, which is described above. TW is used to refer to the number of bits per word as determined by the Transfer Width field (SS10R[9:8]).	000	One word of data is sent at active (falling) edge of FSYNC. The frame period must be at least 8 clocks. Some of the least significant bits of data will not be transmitted if the frame period is less than TW clocks. If the frame period is larger than TW clocks then the remaining output data is padded with the content of SS13R. Most significant bit of SS13R (the Data Pad register) is sent first, and if frame period is larger than TW + 32 clocks then remaining output data is padded with zeros.
		011	Two words of data are sent at active (falling) edge of FSYNC frame. Frame period must be at least 2*TW clocks. If frame period is larger than 2*TW clocks then remaining output data is padded with content of SS13R. Most significant bit of SS13R is sent first, and if frame period is larger than 2*TW + 32 clocks then remaining output data is padded with zeros.
		100	One word of data is sent at beginning of frame and another word of data is sent at middle of frame. The inactive (rising) edge of FSYNC is used to indicate the middle of the frame. Frame period must be at least 8 * TW clocks. Some of the least significant bits of data will not be transmitted if the frame period is less than 2 * TW clocks. In this format, one word of data is sent and, if frame period is larger than 2 * TW, this data is then followed by the most significant word of SS13R. In the middle of the frame, another word of data is sent and, if frame period is larger than 2 * TW, this data is then followed by the least significant word of SS13R. Note that if frame period is less than 2 * TW + 32 clocks then not all bits of SS13R are used; on the other hand, if frame period is larger than 2 * TW + 32 clocks then the remaining bits are filled with zeros.
		101	Two word of data are sent at the beginning of frame and two more words are sent in the middle of frame. In this case inactive (rising) edge of FSYNC is used to indicate middle of frame. In this format, two words of data are sent, and, if frame period is larger than 4 * TW, this data is then followed by the most significant word of SS13R. In the middle of the frame, another two words of data are sent, and, if frame period is larger than 4 * TW, this data is then followed by the least significant word of SS13R. Note that if frame period is less than 4 * TW + 32 clocks then not all bits of SS13R are used; on the other hand, if frame period is larger than 4 * TW + 32 clocks then the remaining bits are filled with zeros
		111	Continuous words of data are sent per frame. Frame period should be a multiple TW clocks, if not the last word transmitted per frame will be cut short in order to sync up with the active (falling) edge of FSYNC.
15	Reserved		

Register 4-177: Codec Transmit Control Register (SS10R: Index 40h, Offset 2C0h)

Bit	Bit Definition	Bit Value	Value Definition
20:16	Codec Transmit FIFO Threshold This parameter indicates the minimum number of empty location, in terms of 16 bit words, in the fifo to generate the Codec Transmit Interrupt.	00000	Reserved.
		00001	Generate Interrupt when FIFO has at least 1 empty location.
		00010	Generate Interrupt when FIFO has at least 2 empty locations.
		00011	Generate Interrupt when FIFO has at least 3 empty locations.
		00100	Generate Interrupt when FIFO has at least 4 empty locations.
		00101	Generate Interrupt when FIFO has at least 5 empty locations.
		00110	Generate Interrupt when FIFO has at least 6 empty locations.
		00111	Generate Interrupt when FIFO has at least 7 empty locations.
		01000	Generate Interrupt when FIFO has at least 8 empty locations.
		01001	Generate Interrupt when FIFO has at least 9 empty locations.
		01010	Generate Interrupt when FIFO has at least 10 empty locations.
		01011	Generate Interrupt when FIFO has at least 11 empty locations.
		01100	Generate Interrupt when FIFO has at least 12 empty locations.
		01101	Generate Interrupt when FIFO has at least 13 empty locations.
		01110	Generate Interrupt when FIFO has at least 14 empty locations.
		01111	Generate Interrupt when FIFO has at least 15 empty locations.
		10000	Generate Interrupt when FIFO has at least 16 empty locations.
		10001	Generate Interrupt when FIFO has at least 17 empty locations.
		10010	Generate Interrupt when FIFO has at least 18 empty locations.
		10011	Generate Interrupt when FIFO has at least 19 empty locations.
		10100	Generate Interrupt when FIFO has at least 20 empty locations.
		10101	Generate Interrupt when FIFO has at least 21 empty locations.
		10110	Generate Interrupt when FIFO has at least 22 empty locations.
		10111	Generate Interrupt when FIFO has at least 23 empty locations.
		11000	Generate Interrupt when FIFO has at least 24 empty locations.
		11001	Generate Interrupt when FIFO has at least 25 empty locations.
		11010	Generate Interrupt when FIFO has at least 26 empty locations.
		11011	Generate Interrupt when FIFO has at least 27 empty locations.
		11100	Generate Interrupt when FIFO has at least 28 empty locations.
		11101	Generate Interrupt when FIFO has at least 29 empty locations.
		11110	Generate Interrupt when FIFO has at least 30 empty locations.
		11111	Generate Interrupt when FIFO has at least 31 empty locations.
23:21	Reserved		

Register 4-177: Codec Transmit Control Register (SS10R: Index 40h, Offset 2C0h)

Bit	Bit Definition	Bit Value	Value Definition
29:24	Codec Transmit FIFO Status (Read Only) This status field indicates the number of filled location in the I^2S Codec Transmit FIFO. This fifo has 32 locations, each location is 16 bits wide and stores one word for transmission. Due to synchronization issues, this field is only valid when transmit is *NOT* enabled.	000000	Transmit FIFO has 0 filled location (fifo empty).
		000001	Transmit FIFO has 1 filled location.
		000010	Transmit FIFO has 2 filled locations.
		000011	Transmit FIFO has 3 filled locations.
		000100	Transmit FIFO has 4 filled locations.
		000101	Transmit FIFO has 5 filled locations.
		000110	Transmit FIFO has 6 filled locations.
		000111	Transmit FIFO has 7 filled locations.
		001000	Transmit FIFO has 8 filled locations.
		001001	Transmit FIFO has 9 filled locations.
		001010	Transmit FIFO has 10 filled locations.
		001011	Transmit FIFO has 11 filled locations.
		001100	Transmit FIFO has 12 filled locations.
		001101	Transmit FIFO has 13 filled locations.
		001110	Transmit FIFO has 14 filled locations.
		001111	Transmit FIFO has 15 filled locations.
		010000	Transmit FIFO has 16 filled locations.
		010001	Transmit FIFO has 17 filled locations.
		010010	Transmit FIFO has 18 filled locations.
		010011	Transmit FIFO has 19 filled locations.
		010100	Transmit FIFO has 20 filled locations.
		010101	Transmit FIFO has 21 filled locations.
		010110	Transmit FIFO has 22 filled locations.
		010111	Transmit FIFO has 23 filled locations.
		011000	Transmit FIFO has 24 filled locations.
		011001	Transmit FIFO has 25 filled locations.
		011010	Transmit FIFO has 26 filled locations.
		011011	Transmit FIFO has 27 filled locations.
		011100	Transmit FIFO has 28 filled locations.
		011101	Transmit FIFO has 29 filled locations.
		011110	Transmit FIFO has 30 filled locations.
		011111	Transmit FIFO has 31 filled locations.
		100000	Transmit FIFO has 32 filled location (FIFO full).
31:30	Reserved		

Register 4-178: Codec Receive Control Register (SS11R: Index 44h, Offset 2C4h)

Bit	Bit Definition	Bit Value	Value Definition
0	Receive Enable	0	Receiver is powered down.
		1	Receiver is enabled.
1	Reset Receive -- This bit is used directly to enable the receive bit clock. SS11R[1] should be held low when changing SS11R[0] from 0 to 1. This will makes sure the receive logic is reset when the Receive bit clock is first started.	0	Codec Receive FIFO is reset, and overflow status (SS01R[23]) is cleared.
		1	Normal operation.
2	Reserved Must be programmed to 0.		
3	Serial Codec Data Input Select I^2S has two serial data inputs one is for the Primary Codec and the other Secondary Codec. This register bit selects which of these inputs is to be used to receive serial data.	0	Receive Codec Data from primary Codec serial input pin, (GPIO44 input).
		1	Receive Codec Data from secondary Codec serial input pin (GPIO65 input). GPIO65 must be configured as input (see the description for the SPI register SPO8R bits 19:18).
5:4	Reserved.		
7:6	Primary serial data in source select This field is used to select the source of data for the primary serial input.	00	Primary serial data comes from the SIN pad. (normal operating mode)
		01	Reserved.
		10	Primary serial data comes from the transmitter output before going to the transmit pad.
		11	Primary serial data comes from the transmitter output after going through the transmit pad.
9:8	Receive Width This field specifies the width of the data to be received.	00	8 bits, receive bits 7-0. FIFO bits 15:8 will be loaded with 2 zeros.
		01	16 bits, receive bits 15-0.
		10	Reserved.
		11	Reserved.
10	Receive Mono Audio This bit is only effective when SS12R[14:12] is set to either 011, 100, or 101.	0	Stereo audio: data received in the beginning of frame and data received in the middle of frame get written to two consecutive fifo locations.
		1	Mono audio: only one sample of data is save in the receive fifo per frame. Whether the sample come from the beginning (left), or middle (right), of the frame is determined by the setting of SS11R[11].
11	Receive Mono Left/Right select This bit is effective only when SS11R[10] is set, and SS11R[14:12] is set to either 011, 100, or 101. In which case the left word is assumed to be the first word received.	0	Receive left only.
		1	Receive right only

Register 4-178: Codec Receive Control Register (SS11R: Index 44h, Offset 2C4h)

Bit	Bit Definition	Bit Value	Value Definition
14:12	Serial Data In Format This parameter specifies the serial data input format. In the below description the width of "word" is determined by the receive width field (SS11R[9:8]), which is described above. RW is used to refer to the number of bits per word as determined by the Receiver Width field.	000	One word of data is captured at beginning of frame. Frame period must be at least RW clocks, or Early Push must be enabled (SS11R[15] = 1) and frame period must be at least 4 clocks.
		011	Two words of data are captured at beginning of frame. Frame period must be at least 2 * RW clocks.
		100	One word of data is captured at beginning of frame and one word of data is captured at the middle of frame. In this case inactive rising edge of FSYNC is used to indicate the middle of the frame. Frame period must be at least 2 * RW clocks, or Early Push must be enabled (SS11R[15] = 1) and frame period must be at least 8 clocks.
		101	Two words of data are captured at beginning of frame and two words of data are captured at the middle of frame. In this case inactive (rising) edge of FSYNC is used to indicate the middle of the frame. Frame period must be at least 4 * RW clocks.
		111	Continuous words of data are captured per frame. Frame period must be a multiple of RW clocks, if not the last word per frame will not get written into the fifo.
		others	Reserved.
15	Early Push Enable This bit should be set if the number of clocks in the FSYNC period is expected to be less than what is needed to transfer receive data. In this case receive data in bit positions that couldn't be received because of the short FSYNC period will be left with zeros. When set this bit enables logic which can generate receive fifo push (s) directly from the output of the FSYNC edge detection logic. Early Push is only effective for Serial Data In Formats (SS11R[14:12] above) 000 and 100.	0	Early Push generation logic disabled.
		1	Early Push generation logic enabled.
21:16	Codec Receive FIFO Threshold This parameter specifies the minimum number of filled location, in terms of 16 bit words, in the Codec Receive FIFO to generate the Codec Receive FIFO Threshold Interrupt. Codec Receive FIFO Threshold interrupt can only be generated if the receiver is enabled (SS11R[0] = 1) and Codec Receive FIFO Threshold Interrupts are enabled (SS01R[6] = 1).	000000	Reserved.
		000001	Interrupt when FIFO has at least one filled location
		000010	Interrupt when FIFO has at least two filled locations
		000011	Interrupt when FIFO has at least three filled locations
		000100	Interrupt when FIFO has at least four filled locations
		000101	Interrupt when FIFO has at least five filled locations
		000110	Interrupt when FIFO has at least six filled locations
		000111	Interrupt when FIFO has at least seven filled locations
		001000	Interrupt when FIFO has at least eight filled locations
		001001	Interrupt when FIFO has at least nine filled locations
		001010	Interrupt when FIFO has at least 10 filled locations
		FIFO values 11-62 are supported	
		111111	Interrupt when FIFO has at least 63 filled locations
23:22	Reserved		

Register 4-178: Codec Receive Control Register (SS11R: Index 44h, Offset 2C4h)

Bit	Bit Definition	Bit Value	Value Definition
30:24	Receive FIFO Status (Read Only) This parameter indicates the number of filled location in the Codec Receive FIFO. This fifo has 64 locations, each location is 16 bits wide and holds one sample of received data. Due to synchronization issues, this field is only valid when transmit is *NOT* enabled.	0000000	Receive FIFO has 0 filled location (fifo empty).
		0000001	Receive FIFO has 1 filled location.
		0000010	Receive FIFO has 2 filled locations.
		0000011	Receive FIFO has 3 filled locations.
		0000100	Receive FIFO has 4 filled locations.
		0000101	Receive FIFO has 5 filled locations.
		0000110	Receive FIFO has 6 filled locations.
		0000111	Receive FIFO has 7 filled locations.
		0001000	Receive FIFO has 8 filled locations.
		0001001	Receive FIFO has 9 filled locations.
		0001010	Receive FIFO has 10 filled locations.
		Register 11 through register 63 are implemented	
		1000000	Receive FIFO has 64 filled locations.
31	Reserved		

The codec FIFO register (see *Register 4-179*) is used to write data to the I^2S Codec Transmit FIFO and to read data from the I^2S Codec Receive FIFO. Data written to this register is pushed into the Codec Transmit FIFO. When Transfer Width is set to 8 bits (SS10R[9:8] = 00), 32, 16 0r 8 bit writes to this register can be used to load the fifo. Because only write data byte zero will actually be used. Likewise when Transfer Width is set to 16 bits (SS10R[9:8] = 01), 32 or 16 bit writes can be used to load the fifo. Only bytes 1 and 0 of the write data will actually be used. Read of this register will return the last data popped from the Codec Receive fifo. After the read the Receive fifo will be popped. The width of the read should be at least as wide as the receive width, SS11R[9:8]. This register should not be written to when Audio Transmit DMA mode is enabled (SS10R[4] = 1).

Register 4-179: Codec FIFO Register (SS12R: Index 48h, Offset 2C8h)

Bit	Bit Definition	Bit Value	Value Definition
15:0	Audio Transmit / Receive Data		
31:16	Reserved		

The data pad register (see *Register 4-180*) outputs additional data to be sent to the external device. This register should only be changed when the Codec transmitter is disabled.

Register 4-180: Codec FIFO Register (SS13R: Index 4Ch, Offset 2CCh)

Bit	Bit Definition	Bit Value	Value Definition
31:0	I^2S Data Pad		Data pad value defines the pattern that is transmitted after FIFO data, when the frame period is larger than what is needed to transmit the data.

Register 4-181: Codec Transmit DMA Buffer-1 Register (SS14R: Index 50h, Offset 2D0h)

Bit	Bit Definition	Bit Value	Value Definition
14:0	Buffer-1 Start Address This parameter specifies the memory address of the 64 bit memory word that is the start of Buffer-1.		
19:15	Reserved		
29:20	Buffer-1 Byte Transfer Count This parameter specifies the number of bytes that are to be read from the Buffer-1 and written to the Codec Transmit FIFO. This count value should be programmed to actual count minus 2, and the least significant bit of the programmed count must be 0. This field allows for a maximum buffer size of 1 Kilobytes. Transfer count must be larger than 32 bytes.		
31:30	Reserved		

Register 4-182: Codec Transmit DMA Buffer-2 Register (SS15R: Index 54h, 2D4h)

Bit	Bit Definition	Bit Value	Value Definition
14:0	Buffer-2 Start Address This parameter specifies the memory address of the 64 bit memory word that is the start of Buffer-2.		
19:15	Reserved		
29:20	Buffer-2 Transfer Count This parameter specifies the number of bytes that are to be read from the Buffer 2 and written to the Codec Transmit FIFO. This count value should be programmed to actual count minus 2; the least significant bit of the programmed count must be 0. This field allows for a maximum buffer size of 1 Kbyte. Transfer count must be larger than 32 bytes.		
31:30	Reserved		

Chapter 5

5-1. DC CHARACTERISTICS

5.2 DC Characteristics - Tables and Specifications

Table 5-1, "Absolute Maximum Conditions", through *Table* 5-4, "DC Characteristics", describe the DC characteristics and operating conditions.

TABLE 5-1: Absolute Maximum Conditions

Symbol	Parameter	Minimum	Maximum	Units
V_{CCCORE}	Supply Voltage for the internal Core	-0.5	2.3	V
V_{CC}	Supply Voltage for I/O	-0.5	3.6	V
V_I	Input Voltage for I/O	-0.5	3.6	V
T_{STG}	Storage Temperature	-40	125	°C

Note: *Permanent device damage may occur if the specifications for the Absolute Maximum Conditions are exceeded. All voltages are defined with respect to ground.*

Operation of the MQ-1100/1132 device must be restricted to normal operating conditions. These are specified in *Table 5-2*.

TABLE 5-2: Normal Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{CCCORE}	Internal core supply voltage	1.71	1.8	1.89	V
V_{CC}	I/O pin supply voltage	3.0	3.3	3.6	V
T_A	Ambient temperature	0	—	70	°C

Power dissipation for various functions of the MQ-1100 and the MQ-1132 devices is specified in *Table* 5-3, "Power Dissipation by Function". Wattage is uniquely specified for each function.

TABLE 5-3: Power Dissipation by Function

Function	Power Dissipation (Typical)	Units
Graphics [1]	30	mW
USB Device [2]	5.0	mW
USB Host [3] (MQ-1132 only)	0.4	mW
Serial Peripheral Interface [4] (MQ-1132 only)	0.5	mW
Audio Codec Interface [5] (MQ-1132 only)	2.5	mW

1. This includes the memory controller running at 24 MHz, graphics controller running at 6.4 MHz, SRAM, flat panel interface and CPU interface (running at 48 MHz). This assumes a 320 x 240 x 16bpp TFT panel based system running full speed graphic updates with graphics engine active running at 24 MHz.
2. This includes the internal USB transceiver and assumes full speed continuous transfers.
3. This includes the internal USB transceiver and assumes attached low speed device (mouse)
4. This assumes a one MHz operation (touch panel controller)
5. This assumes playback at 44.1 kHz sampling and 11.2896 MHz.

TABLE 5-4: DC Characteristics [1]

Symbol	Parameter	Notes	Minimum	Maximum	Units
P_D	Power dissipation	_	_	_	_
I_{IL}	Input low leakage current	Input-only pins (non-SPI)	_	1.0	µA
		SPI pins (GPIO[53:50]) [2]	_	0.25	µA
		Bi-directional pins	_	1.0	µA
I_{IH}	Input high leakage current	Input-only pins (non-SPI)	_	1.0	µA
		SPI pins (GPIO[53:50])	_	0.25	µA
		Bi-directional pins	_	1.0	µA
I_{OZL}	Output low impedance leakage current	All I/O pins	_	1.0	µA
I_{OZH}	Output high impedance leakage current	All I/O pins	_	-1.0	µA
V_{IL}	Input low voltage	SPI	0.0	$0.2 \times V_{CC}$	V
		All inputs other than SPI	0.0	0.7	V
V_{IH}	Input high voltage	SPI	$0.7 \times V_{CC}$	V_{CC}	V
		USB (single ended)	2.0	V_{CC}	V
		All inputs other than USB (single ended) and SPI	2.5	V_{CC}	V
V_{OL} (@ 4mA load)	Output low voltage	All outputs	0.0	0.5	V
V_{OH} (@ 4mA load)	Output high voltage	SPI (-1.0 mA)	$0.8 \times V_{CC}$	V_{CC}	V
		All outputs other than SPI	2.8	V_{CC}	V

1. Values at nominal voltage
2. SPI pins GPIO50, GPIO51, GPIO52, and GPIO53 are represented by BGA package balls N4, N3, L3, and L1, respectively.

Chapter 6

6-1. AC Timing Characteristics

This chapter describes the AC characteristics of the MQ-1100/1132 LCD and Peripheral Controller device.

The AC characteristics consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of other signals. All timing specifications correspond to an operating frequency (see the Table footnotes) and an operating supply voltage from V_{DDMIN} to V_{DDMAX} under an operating temperature from T_L to T_H.

Figure 6-1 illustrates the read cycle timing waveform for the Motorola Dragonball. *Table 6-1* specifies the timing measurements in the figure.

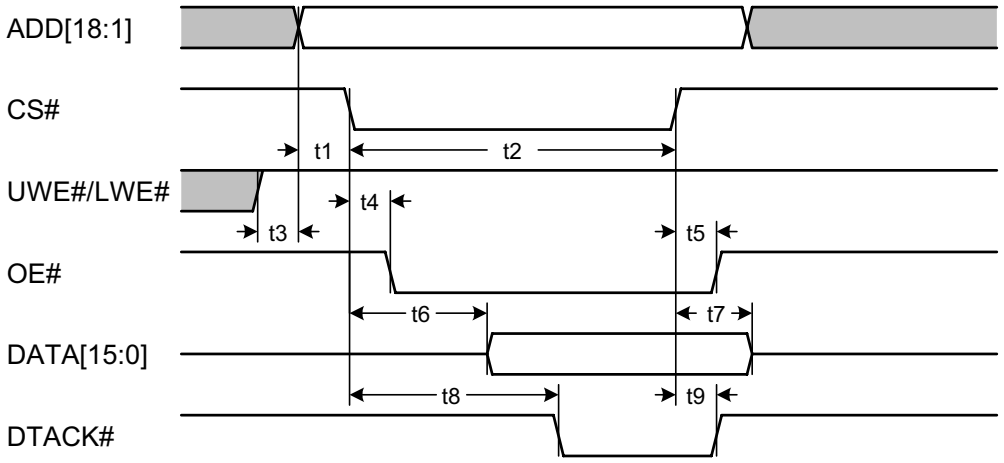


Figure 6-1 Motorola Dragonball Read

TABLE 6-1: Motorola Dragonball Read [1] [2] [3]

Number	Parameter	Minimum	Maximum	Units
t1	Address valid to CS# asserted	20	—	ns
t2	CS# pulse width	(60+T/2)+nT	—	ns
t3	UWE#/LWE# negated before address valid	0	—	ns
t4	CS# asserted to OE# asserted	—	0	ns
t5	OE# negated after CS# negated	0	10	ns
t6	Data-in valid from CS# asserted	—	35+nT	ns
t7	Data-in hold after CS# negated	0	—	ns
t8	DTACK# input setup from CS# asserted	—	20+nT	ns
t9	DTACK# input hold after CS# negated	0	—	ns

1. *n* is the number of wait-states in the current memory access cycle.
2. *T* is the system clock period; Tmin = 33MHz
3. The external $\overline{\text{DTACK}}$ input requirement is eliminated when $\overline{\text{CSx}}$ is programmed to use the internal $\overline{\text{DTACK}}$. $\overline{\text{CSx}}$ represents $\overline{\text{CSA0}}$, $\overline{\text{CSA1}}$, $\overline{\text{CSB0}}$, $\overline{\text{CSB1}}$, $\overline{\text{CSC0}}$, $\overline{\text{CSC1}}$, $\overline{\text{CSD0}}$, or $\overline{\text{CSD1}}$.

Figure 6-2 illustrates the write cycle timing waveform for the Motorola Dragonball. *Table 6-2* specifies the timing measurements in the figure.

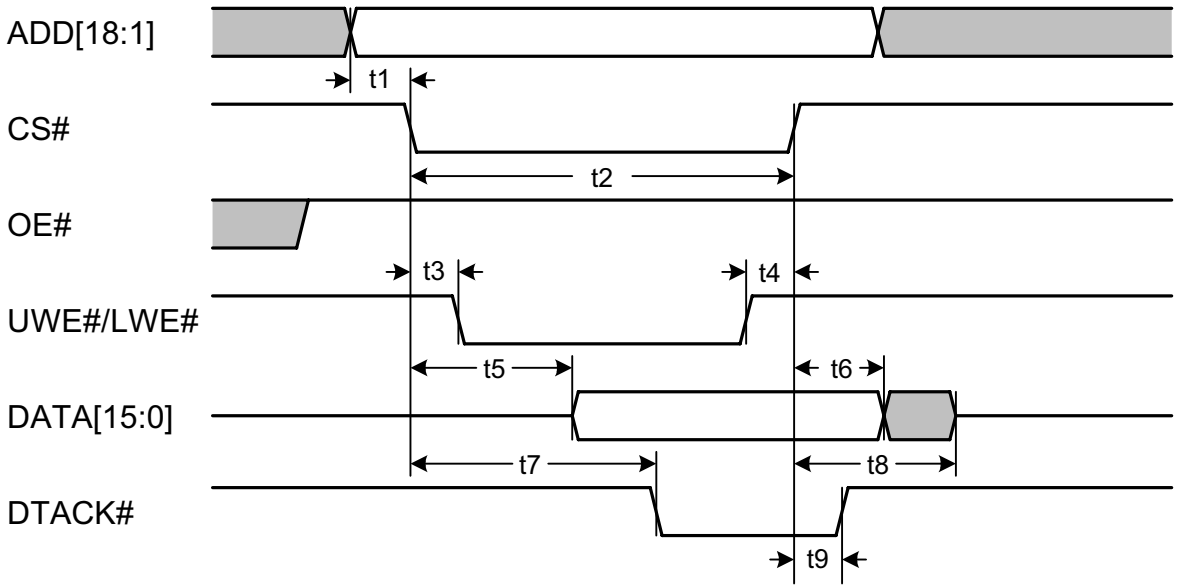


Figure 6-2 Motorola Dragonball Write

TABLE 6-2: Motorola Dragonball Write [1] [2] [3]

Number	Parameter	Minimum	Maximum	Units
t1	Address valid to CS# asserted	20	—	ns
t2	CS# pulse width	(60+T/2) +nT	—	ns
t3	CS# asserted to UWE#/LWE# asserted	0	4	ns
t4	UWE#/LWE# negated before CS# negated	10	20	ns
t5	CS# asserted to data-out valid	—	30	ns
t6	Data-out hold after CS# negated	8	—	ns
t7	DTACK# input setup from CS# asserted	—	20 +nT	ns
t8	CS# negated to data-out in Hi-Z	—	18	ns
t9	DTACK# input hold after CS# negated	0	—	ns

1. *n* is the number of wait-states in the current memory access cycle.
2. *T* is the system clock period; *T* min = 33MHz
3. The external $\overline{\text{DTACK}}$ input requirement is eliminated when $\overline{\text{CSx}}$ is programmed to use the internal $\overline{\text{DTACK}}$. $\overline{\text{CSx}}$ represents $\overline{\text{CSA0}}$, $\overline{\text{CSA1}}$, $\overline{\text{CSB0}}$, $\overline{\text{CSB1}}$, $\overline{\text{CSC0}}$, $\overline{\text{CSC1}}$, $\overline{\text{CSD0}}$, or $\overline{\text{CSD1}}$.

Figure 6-3 illustrates the read cycle timing waveform for the Intel SA11xx. *Table 6-3* specifies the timing measurements in the figure.

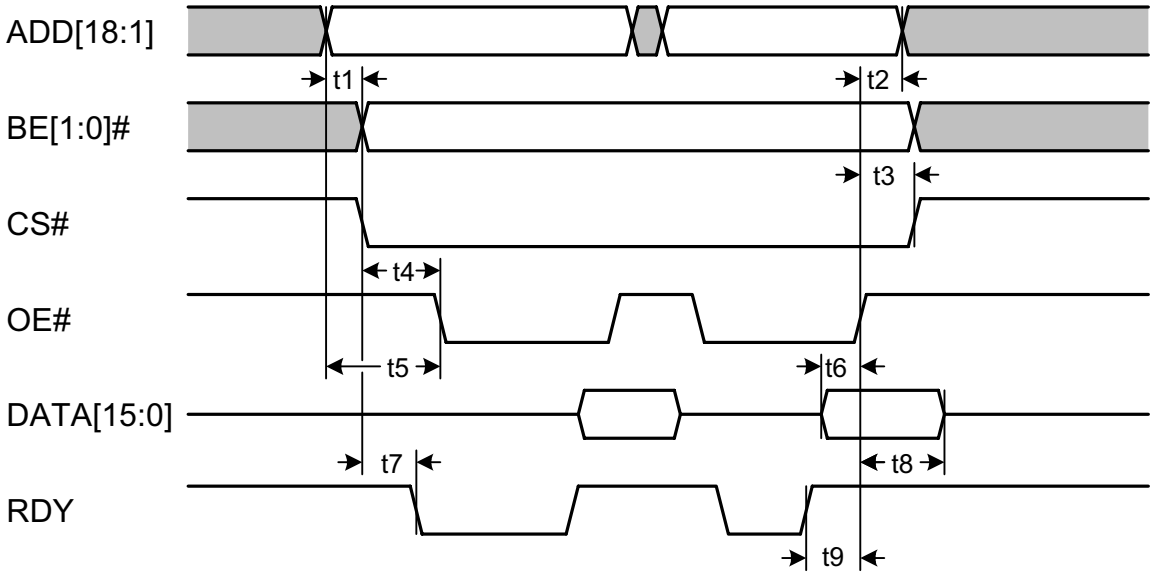


Figure 6-3 Intel SA11xx Read

TABLE 6-3: Intel SA11xx Read [1]

Number	Parameter	Minimum	Maximum	Units
t1	Address setup to CS# asserted	5	—	ns
t2	Address hold from OE# negated	5	—	ns
t3	OE# negated to CS# negated	—	10	ns
t4	CS# asserted to OE# asserted	20	—	ns
t5	Address setup to OE# asserted	25	—	ns
t6	Data-in setup to OE# negated	20	—	ns
t7	CS# asserted RDY negated	—	15	ns
t8	Data-in hold from OE# negated	0	—	ns
t9	RDY asserted to OE# negated	25	—	ns

1. Minimum system clock period = 12 ns (83MHz)

Note: *Higher system clock frequency operation is supported. Contact MediaQ for information on timing and formulas for calculating the correct CPU bus states.*

Figure 6-4 illustrates the write cycle timing waveform for the Intel SA11xx. *Table 6-4* specifies the timing measurements in the figure.

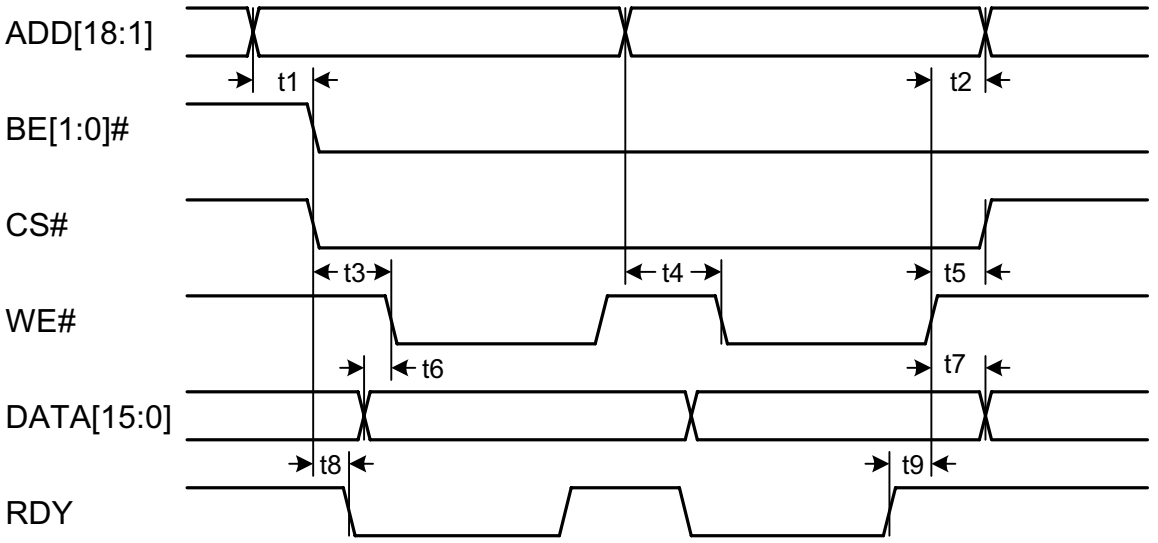


Figure 6-4 Intel SA11xx Write

TABLE 6-4: Intel SA11xx Write [1]

Number	Parameter	Minimum	Maximum	Units
t1	Address setup to CS# asserted	5	—	ns
t2	Address hold from WE# negated	5	—	ns
t3	CS# asserted to WE# asserted	20	20	ns
t4	Address setup to WE# asserted	25	—	ns
t5	WE# negated to CS# negated	—	10	ns
t6	Data-out setup to WE# negated	20	—	ns
t7	Data-out hold from WE# negated	5	—	ns
t8	CS# asserted to RDY negated	—	15	ns
t9	RDY asserted to WE# negated	25	—	ns

1. Minimum system clock period = 12 ns (83MHz)

Note: *Higher system clock frequency operation is supported. Contact MediaQ for information on timing and formulas for calculating the correct CPU bus states.*

Figure 6-5 illustrates the read cycle timing waveform for the NEC 41xx. *Table 6-5* specifies the timing measurements in the figure.

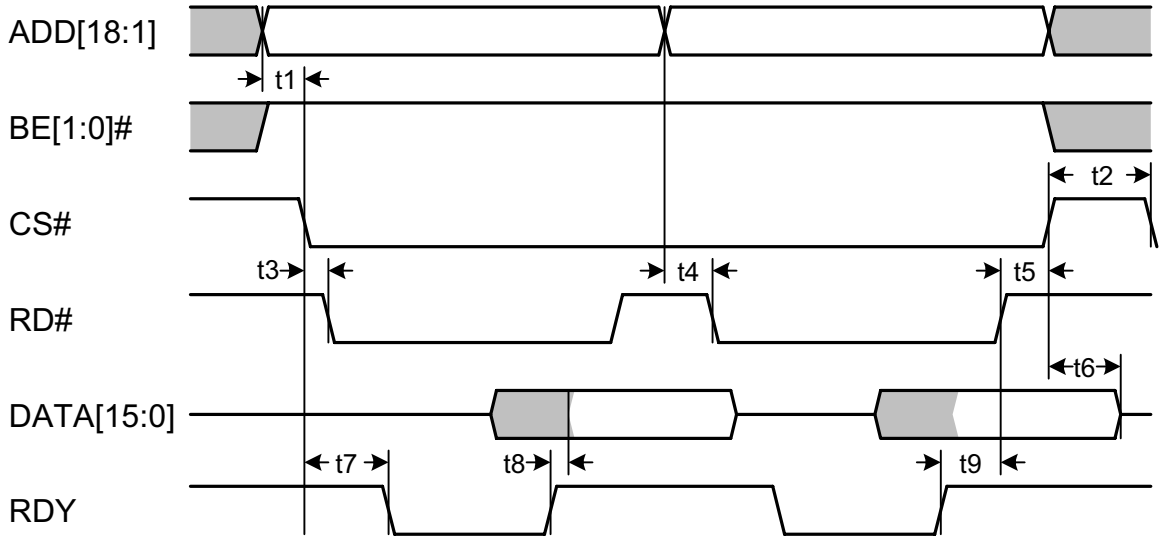


Figure 6-5 NEC 41xx Read

TABLE 6-5: NEC 41xx Read [1]

Number	Parameter	Minimum	Maximum	Units
t1	Address valid to CS# asserted	0	—	ns
t2	CS# negated to next CS# asserted	50	—	ns
t3	CS# asserted to RD# asserted	15	100	ns
t4	Address valid to RD# asserted	15	—	ns
t5	RD# negated to CS# negated	—	50	ns
t6	Data-in hold from CS# negated	0	—	ns
t7	CS# asserted to RDY negated	—	15	ns
t8	RDY asserted to Data-out valid	—	30	ns

1. Minimum system clock period = 50 ns (20MHz)

Figure 6-6 illustrates the write cycle timing waveform for the NEC 41xx. *Table 6-6* specifies the timing measurements in the figure.

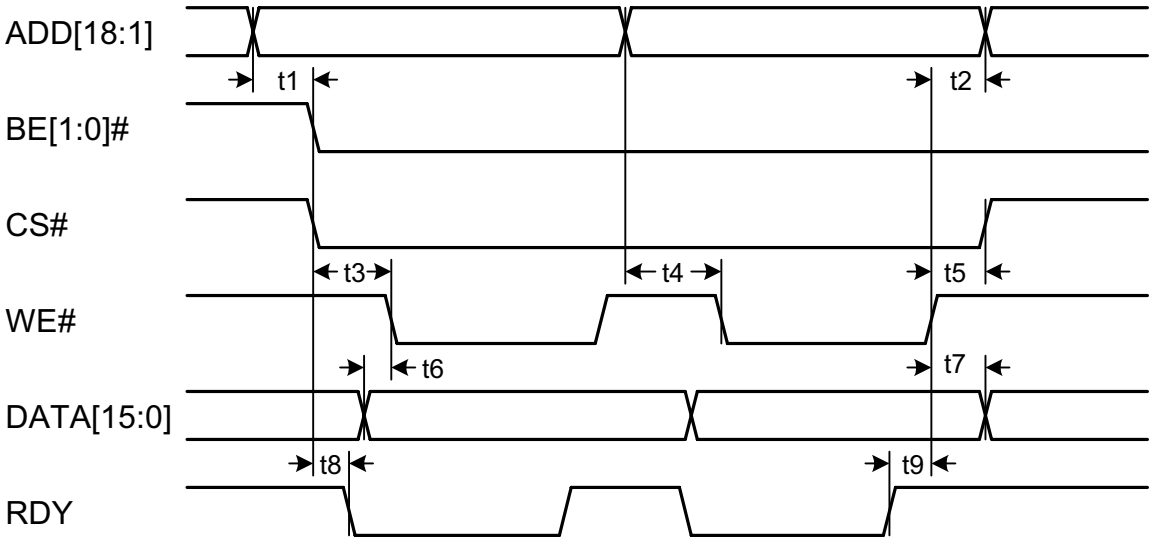


Figure 6-6 NEC 41xx Write

TABLE 6-6: NEC 41xx Write [1]

Number	Parameter	Minimum	Maximum	Units
t1	Address valid to CS# asserted	0	—	ns
t2	Byte enable setup to WE# asserted	15	—	ns
t3	CS# asserted to WE# asserted	15	—	ns
t4	Address valid to WE# asserted	15	—	ns
t5	Data-out setup to WE# asserted	15	—	ns
t6	WE# negated to CS# negated	—	50	ns
t7	CS# asserted to RDY negated	—	15	ns

1. Minimum system clock period = 50 ns (20MHz)

Figure 6-7 illustrates the read cycle timing waveform for the Hitachi SH 7750. *Table 6-7* specifies the timing measurements in the figure.

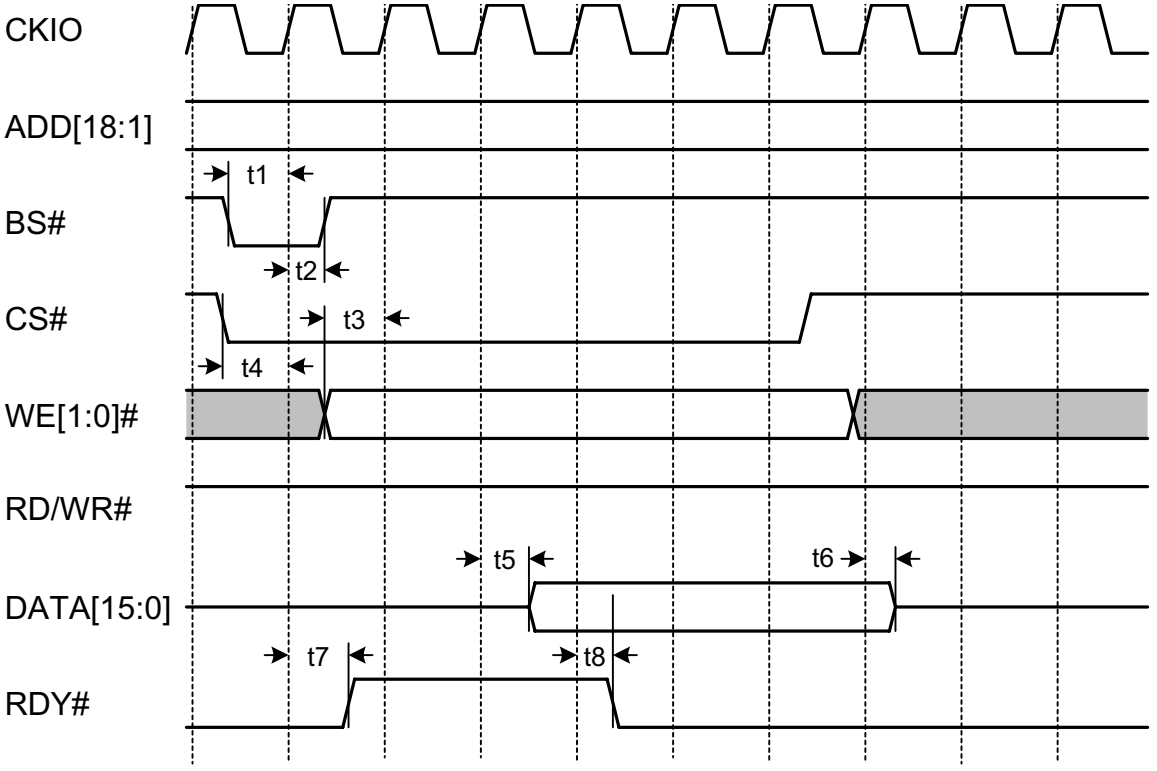


Figure 6-7 Hitachi SH 7750 Read

TABLE 6-7: Hitachi SH 7750 Read [1]

Number	Parameter	Minimum	Maximum	Units
t1	BS# setup time	5	—	ns
t2	BS# hold time	0	—	ns
t3	WE# setup time	5	—	ns
t4	CS# setup time	5	—	ns
t5	Data valid delay	—	18	ns
t6	Data invalid delay	0	—	ns
t7	Delay to RDY# negated	—	12	ns
t8	Delay to RDY# asserted	—	12	ns

1. CKIO min = 15 ns (66MHz)

Figure 6-8 illustrates the write cycle timing waveform for the Hitachi SH 7750. *Table 6-8* specifies the timing measurements in the figure.

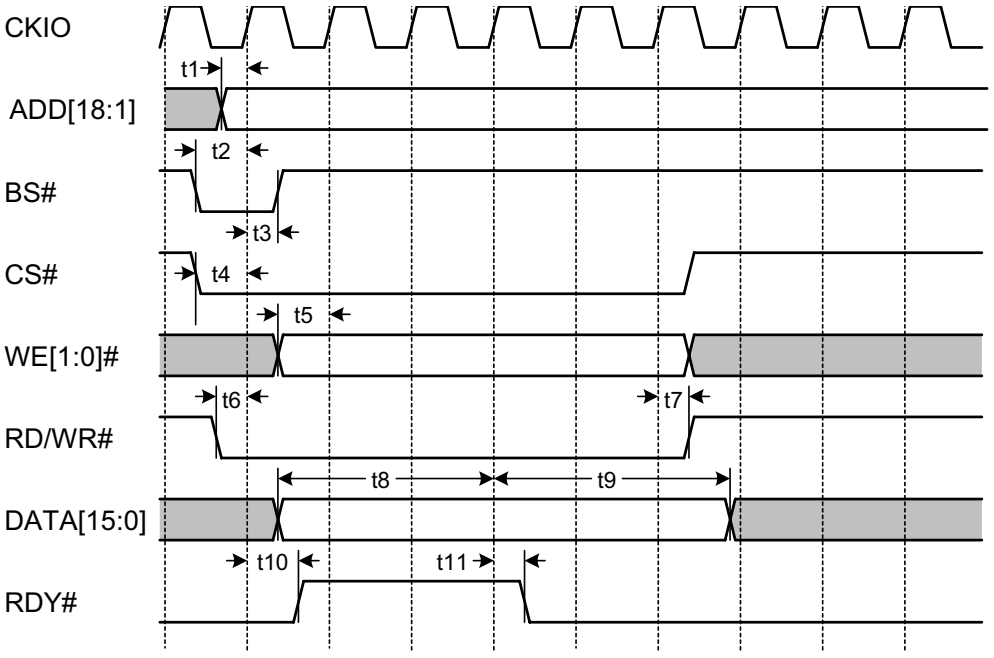


Figure 6-8 Hitachi SH 7750 Write

TABLE 6-8: Hitachi SH 7750 Write [1]

Number	Parameter	Minimum	Maximum	Units
t1	Address setup time	5	—	ns
t2	BS# setup time	5	—	ns
t3	BS# hold time	0	—	ns
t4	CS# setup time	5	—	ns
t5	WE# setup time	5	—	ns
t6	RD/WR# setup time	5	—	ns
t7	RD/WR# hold time	3	—	ns
t8	Data setup time	10	—	ns
t9	Data hold time	10	—	ns
t10	Delay to RDY# negated	—	12	ns
t11	Delay to RDY# asserted	—	12	ns

1. CKIO min = 15 ns (66MHz)

Figure 6-9 illustrates the read cycle timing waveform for the Hitachi SH 7709. *Table 6-9* specifies the timing measurements in the figure.

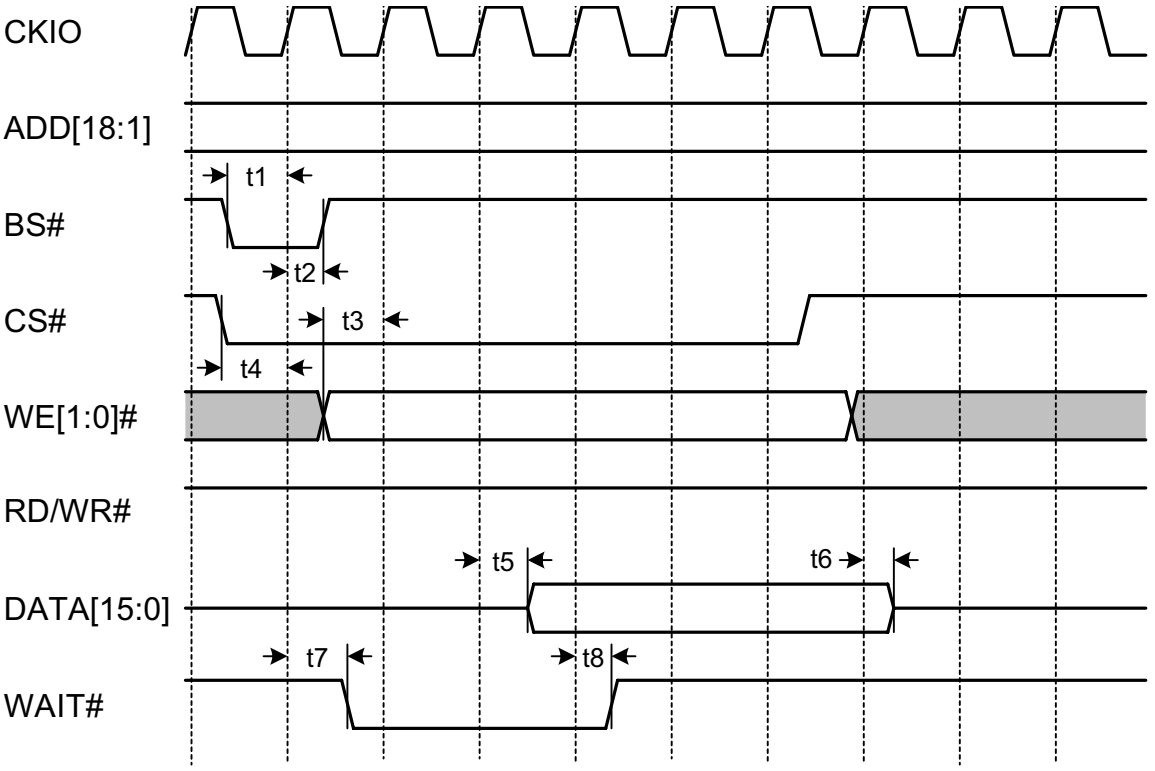


Figure 6-9 Hitachi SH 7709 Read

TABLE 6-9: Hitachi SH 7709 Read [1]

Number	Parameter	Minimum	Maximum	Units
t1	BS# setup time	5	—	ns
t2	BS# hold time	0	—	ns
t3	WE# setup time	5	—	ns
t4	CS# setup time	5	—	ns
t5	Data valid delay	—	18	ns
t6	Data invalid delay	0	—	ns
t7	Delay to WAIT# asserted	—	12	ns
t8	Delay to WAIT# negated	—	12	ns

1. CKIO min = 15 ns (66MHz)

Figure 6-9 illustrates the write cycle timing waveform for the Hitachi SH 7709. *Table 6-10* specifies the timing measurements in the figure.

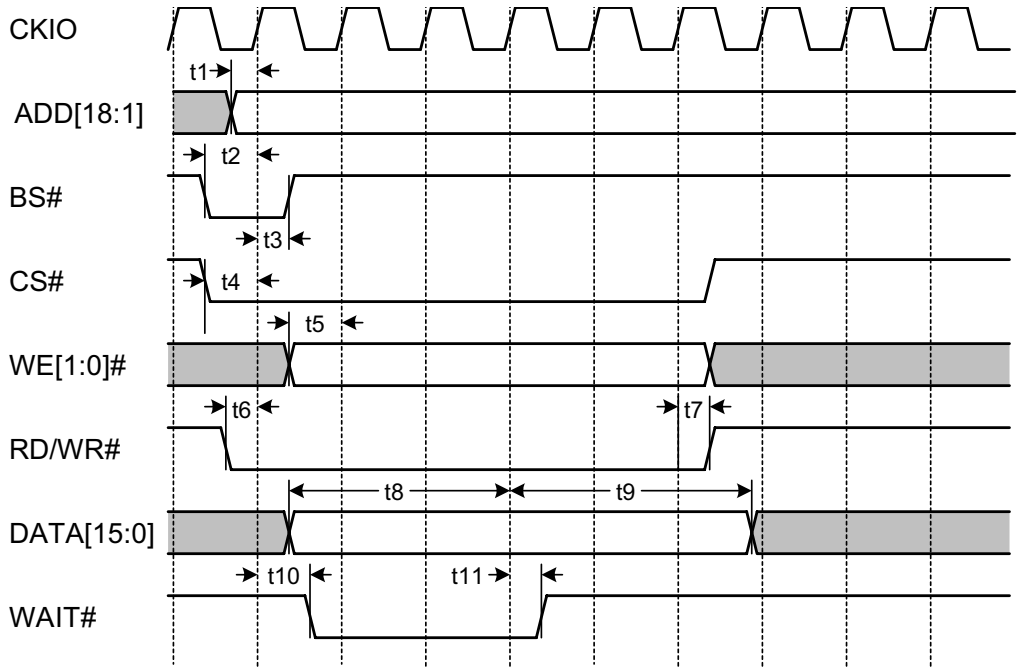


Figure 6-10 Hitachi SH 7709 Write

TABLE 6-10: Hitachi SH 7709 Write [1]

Number	Parameter	Minimum	Maximum	Units
t1	Address setup time	5	—	ns
t2	BS# setup time	5	—	ns
t3	BS# hold time	0	—	ns
t4	CS# setup time	5	—	ns
t5	WE# setup time	5	—	ns
t6	RD/WR# setup time	5	—	ns
t7	RD/WR# hold time	3	—	ns
t8	Data setup time	10	—	ns
t9	Data hold time	10	—	ns
t10	Delay to WAIT# asserted	—	12	ns
t11	Delay to WAIT# negated	—	12	ns

1. CKIO min = 15 ns (66MHz)

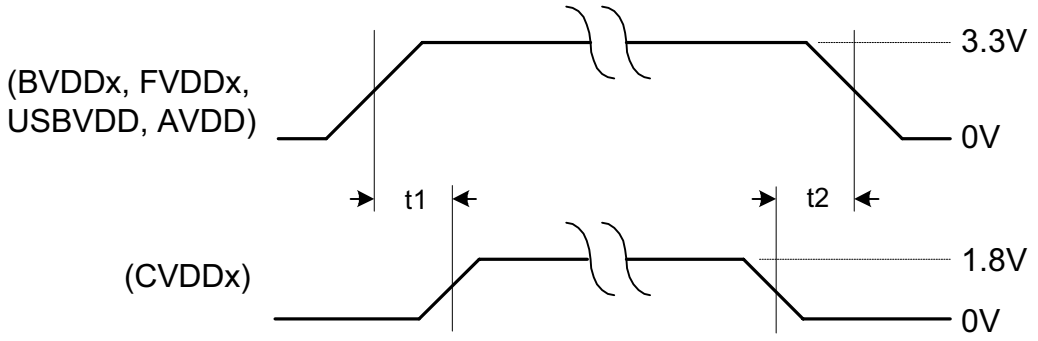


Figure 6-11 MQ-1100/1132 Power Sequencing

TABLE 6-11: MQ-1100/1132 Power Sequencing [1]

Number	Parameter	Minimum	Maximum	Units
t1	3.3V (BVDDx, FVDDx, USBVDD, VDDOSC) applied to 1.8V (CVDDx) applied delay	0	1	ms
t2	1.8V (CVDDx) removal to 3.3V (BVDDx, FVDDx, USBVDD, VDDOSC) removal delay	0	1	ms

1. These specifications are recommendations and damage should not occur; even if the 1.8V supply is applied first for a brief period of time (<1ms). However, this condition is not guaranteed by MediaQ's test program and should be avoided whenever possible.